Effective Power/Ground Plane Decoupling for PCB

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Power Plane Noise Control

“Ground Bounce”
Power/Ground-Reference Plane Noise

• Must consider TWO Major Factors
  – EMC -- Reduce noise along edge of board from IC somewhere else
  – Functionality -- Provide IC with sufficient charge
• Decoupling strategies are FULL of **Myths**
  – Consider the physics
  – Don’t forget **Inductance!**
Source of Power/Ground-Reference Plane Noise

- Power requirements from IC during switching
- Critical Net currents routed through via
Power Bus Spectrum
Clock Driver IDT74FCT807
Noise Injected between Planes Due to Critical Net Through Via

FR4 $\varepsilon_r=4.2$  Loss $\tan=0.02$
Transfer Function from Via to I/O Pin

Transfer Function From Via-to-Via
20x30cm Board

- Frequency (Hz)
- Transfer Function (dB)

- 5 mil Separation
- 10 mil Separation
- 15 mil Separation
- 25 mil Separation
- 35 mil Separation

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Decoupling Must be Analyzed in Different Ways for Different Functions

• EMC
  – Resonance big concern
  – Requires STEADY-STATE analysis
    • Frequency Domain
  – Transfer function analysis
    • Eliminate noise along edge of board due to ASIC/IC located far away
Decoupling Must be Analyzed in Different Ways for Different Functions

• Provide Charge to ASIC/IC
  – Requires TRANSIENT analysis
  – Charge will NOT travel from far corners of the board fast enough
  – Local decoupling capacitors dominate
  – Impedance at ASIC/IC pins important
Steady-State Analysis

- Measurements and Simulations
- Test Board with Decoupling capacitors every 1” square
Test Board Ports

Figure 1

Test Board Ports

#1 #2 #3 #4 #5
#6 #7 #8 #9 #10
#11 #12 #13 #14 #15
S21 Used for Decoupling “Goodness”

- Ratio of Power ‘out’ to power ‘in’
- Better Indicator of EMI noise transmission across board
- Also used to validate simulations
Measured $S_{21}$ for 12" x 10" PC Board Between Power/Ground Planes with No Decoupling Capacitors (Measured Center to Corner)

- Board Capacitance Dominates
- Physical Board Size Resonances Dominate
Test Board Decoupling Capacitor Placement for 25 .01 uf Caps

<table>
<thead>
<tr>
<th>Possible Cap Location</th>
<th>Populated Cap Locations</th>
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<tr>
<td><img src="image-url" alt="Diagram" /></td>
<td><img src="image-url" alt="Diagram" /></td>
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</table>
Test Board Decoupling Capacitor Placement for 51 .01 uf Caps
Measured $S_{21}$ for 12" x 10" PC Board Between Power/Ground Planes with Various Amounts of Decoupling Capacitors (Measured Center to Corner)
S21 Between Port #8 and Port #1 on Test Board
With Various Amounts of .01 uf Decoupling Capacitors

No Caps
25 Caps
51 Caps
99 Caps
Cap Impedance

- 0.01uF
- 22pF
- 0.01uF in parallel with 22pF

|Z| (Ohms)

Freq (Hz)
Test Board Decoupling Capacitor Placement
for 41 22pf Caps
(In Addition to 99 .01uf Caps)

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<tr>
<th>Possible Cap Location</th>
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S21 Between Port #8 and Port #1 on Test Board
With 99 .01 uf Decoupling Capacitors and Various Amounts of 22pf Capacitors Added

![Graph showing S21 (dB) vs Frequency (Hz) for different numbers of 22pf capacitors.]

- 9 22pf Caps
- 17 22pf Caps
- 21 22pf Caps
- 33 22pf Caps
- 41 22pf Caps
- 99 22pf Caps
- 99 Caps

Frequency (Hz)

S21 (dB)
Measured Comparison of Multiple and Single Value Decoupling Capacitor Strategies

-90
-80
-70
-60
-50
-40
-30
-20
-10
0

0.0E+00 2.0E+08 4.0E+08 6.0E+08 8.0E+08 1.0E+09 1.2E+09 1.4E+09 1.6E+09 1.8E+09

Frequency (Hz)

S21 Transfer Function (dB)

No Caps
99 0.01 uF Caps
0.01 uF and 330 pF Caps
Comparison of Model and Measured Data
for 10" x 12" Board
99 caps -- alternating .01uF and 330pF

S21 (dB)

Frequency (Hz)
Voltage Distribution @ 350 MHz .01uF and 330pF Case (Source in Center)
Voltage Distribution @ 750 MHz
.01uF and 330pF Case (Source in Center)
Voltage Distribution @ 950 MHz
.01uF and 330pF Case (Source in Center)
Decoupling Capacitor Mounting

- Keep as to planes as close to capacitor pads as possible

Inductance Depends on Loop $\text{AREA}$

Via Separation

Height above Planes
Decoupling Capacitor Mounting

- Keep as to planes as close to capacitor pads as possible
Via Configuration Can Change Inductance

The “Good”

The “Bad”

The “Ugly”

Really “Ugly”

SMT Capacitor
Via
Capacitor Pads

Best
Better

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Comparison of Decoupling Capacitor Impedance
100 mil Between Vias & 10 mil to Planes

<table>
<thead>
<tr>
<th>Impedance (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000pF</td>
</tr>
<tr>
<td>0.01uF</td>
</tr>
<tr>
<td>0.1uF</td>
</tr>
<tr>
<td>1.0uF</td>
</tr>
</tbody>
</table>

Frequency (Hz)

10^6 10^7 10^8 10^9 10^10
Comparison of Decoupling Capacitor Via Separation Distance Effects

0.1 uF Capacitor

<table>
<thead>
<tr>
<th>Via Separation (mils)</th>
<th>Inductance (nH)</th>
<th>Impedance @ 1 GHz (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>.06</td>
<td>.41</td>
</tr>
<tr>
<td>40</td>
<td>0.21</td>
<td>1.3</td>
</tr>
<tr>
<td>60</td>
<td>0.36</td>
<td>2.33</td>
</tr>
<tr>
<td>80</td>
<td>0.5</td>
<td>3.1</td>
</tr>
<tr>
<td>100</td>
<td>0.64</td>
<td>4.0</td>
</tr>
<tr>
<td>150</td>
<td>1.0</td>
<td>6.23</td>
</tr>
<tr>
<td>200</td>
<td>1.4</td>
<td>8.5</td>
</tr>
<tr>
<td>300</td>
<td>2.1</td>
<td>12.69</td>
</tr>
<tr>
<td>400</td>
<td>2.75</td>
<td>17.3</td>
</tr>
<tr>
<td>500</td>
<td>3.5</td>
<td>21.7</td>
</tr>
</tbody>
</table>
# Example Connection Inductance Values

<table>
<thead>
<tr>
<th>Spacing between Vias</th>
<th>Complex Formula (20 mils to plane)</th>
<th>Simple rect loop (20 mils to plane)</th>
<th>Complex Formula (10 mils to plane)</th>
<th>Simple rect loop (10 mils to plane)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0805 + 2*10mil</td>
<td>3.0 nH</td>
<td>3.1 nH</td>
<td>2 nH</td>
<td>1.38 nH</td>
</tr>
<tr>
<td>0805 + 2*100mil</td>
<td>4.1 nH</td>
<td>4.3 nH</td>
<td>3 nH</td>
<td>2.0 nH</td>
</tr>
<tr>
<td>0805 + 2*160mil</td>
<td>5.1 nH</td>
<td>5.1 nH</td>
<td>3.5 nH</td>
<td>2.5 nH</td>
</tr>
<tr>
<td>0603 + 2*10mil</td>
<td>2.3 nH</td>
<td>1.74 nH</td>
<td>1.1 nH</td>
<td>0.8 nH</td>
</tr>
<tr>
<td>0603 + 2*100mil</td>
<td>3.3 nH</td>
<td>3.15 nH</td>
<td>2.1 nH</td>
<td>1.5 nH</td>
</tr>
<tr>
<td>0603 + 2*160mil</td>
<td>4.2 nH</td>
<td>4.3 nH</td>
<td>2.4 nH</td>
<td>2.07 nH</td>
</tr>
</tbody>
</table>

Sources for complex formula:


Transient Analysis
(Time Limited)

- Provide charge to ASIC/IC
- Inductance dominates impedance
  - Loop area 1st order effect
- Traditional analysis not accurate enough
Current in IC During Logic Transitions (CMOS)

- During logic 0-1 transition, charge current flows through the IC driver and load, causing a shoot-through current.
- During logic 1-0 transition, discharge current flows through the IC driver and load, again causing a shoot-through current.

Diagrams illustrate the charge and discharge currents during logic transitions.
Typical PCB Power Delivery

- DC/DC converter (Power source)
  - SMT capacitors
  - IC driver
  - Electrolytic capacitor
  - IC load
Equivalent Circuit for Power Current Delivery to IC

- $V_{DC}$
- Connector and wiring
- Capacitor leads
- Via interconnect
- PCB wiring
- DC/DC converter
- Electrolytic capacitors
- SMT capacitors
- $V_{CC}/GND$ plane
- IC load
- Switch
Traditional Analysis #1

• Use impedance of capacitors in parallel

![Diagram showing impedance analysis with capacitors and ESL values.]

No Effect of Distance Between Capacitors and IC Included!
Traditional Impedance Calculation for Four Decoupling Capacitor Values

Impedance (ohms) vs Frequency (Hz)

- .1uF
- .01uF
- .001uF
- .0001uF
- All in Parallel
Traditional Analysis #2

- Calculate loop area – Traditional loop inductance formulas
  - Which loop area? Which size conductor

Over Estimates L and Ignores Distributed Capacitance
More Accurate Model Includes Distributed Capacitance
Distributed Capacitance Schematic

- Intentional Capacitor
- Distributed Capacitance
- ESR
- Loop L
- Capacitance

Note: L increases as distance from source increases
Effect of Distributed Capacitance

- Can NOT be calculated/estimated using traditional capacitance equation
- Displacement current amplitude changes with position and distance from the source
Displacement Current
500 MHz via @450 mils from Source
Need to Find the Real Effect of Decoupling Capacitor Distance

- Perfect decoupling capacitor is a via between planes
- FDTD simulation to find the effect of shorting via distance from source
- Vary spacing between planes, distance to via, frequency, etc
Impedance of Shorting Via vs. Frequency
Four Via Case (20 mil Separation Between Plates)
Impedance Result

- Linear with frequency (on log scale)
- Looks like an inductance only!
- Consider this inductance an **Apparent Inductance**
- Apparent inductance is constant with frequency
Apparent Inductance for One Shorting Via Case
20 mil Plate Separation

![Graph showing inductance vs frequency for different plate separations.](image-url)
Formulas to Predict Apparent Inductance

\[ L_{\text{one–via}} = (0.1336s - 0.0654)\ln(dist) + (-0.2609s + 0.2675) \]
\[ L_{\text{two–via}} = (0.1307s - 0.0492)\ln(dist) + (-0.2948s + 0.1943) \]
\[ L_{\text{three–via}} = (0.1242s - 0.0447)\ln(dist) + (-0.2848s + 0.1763) \]
\[ L_{\text{four–via}} = (0.1192s - 0.0403)\ln(dist) + (-0.2774s + 0.1592) \]

\( s = \text{separation between plates (mils/10)} \)
\( dist = \text{distance to via} \)
True Impedance for Decoupling Capacitor

IC Capacitor

Power
Gnd

L_{IC}

L_{apparent}

L_{cap}

Source

ESR

L_{cap} + L_{IC}

Nominal Capacitance
Impedance Calculation with Apparent Inductance for Four Decoupling Capacitor Values

<table>
<thead>
<tr>
<th>Cap Value</th>
<th>Distance to Cap from IC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 uF</td>
<td>800mils 1200mils 1500mils</td>
</tr>
<tr>
<td>0.01 uF</td>
<td>600mils 900mils 1100mils</td>
</tr>
<tr>
<td>0.001uF</td>
<td>400mils 700mils 800mils</td>
</tr>
<tr>
<td>0.0001uF</td>
<td>200mils 400mils 400mils</td>
</tr>
</tbody>
</table>

Frequency (Hz)

Impedance (ohms)
Effect of Distributed Capacitance

- Can NOT be calculated/estimated using traditional capacitance equation
- Displacement current amplitude changes with position and distance from the source
- Following examples use cavity resonance technique (EZ-PowerPlane)
  - Frequency Domain to compare to measurements
  - Time Domain using SPICE circuit from cavity resonance analysis
Parameters for Comparison to Measurements

- Dielectric thickness = 35 mils
- Dielectric constant = 4.5, Loss tan = 0.02
- Copper conductivity = $5.8 \times 10^7$ S/m
Measured vs Model (MoM) S21 for 12" x 10" PC Power/gnd
with 25 .01uF caps
Position 8-to-1

S21 (dB)

Frequency (Hz)

No Caps - Measured
EZ-PP No Caps
Measured vs Model (EZ-PP) S21 for 12" x 10" PC Power/gnd with 25 .01uF caps
Position 8-to-1
Measured vs Model (EZ-PP) S21 for 12" x 10" PC Power/gnd with 95 .01uF caps
Position 8-to-1
Impedance at Port #1
Single 0.01 uF Capacitor at Various Distances (35mil Dielectric)
Z11 Phase Comparison as Capacitor distance Varies for 35 mils FR4
ESL = 0.5nH

Frequency (Hz)

Phase (rad)

100 mils
200 mils
300 mils
400 mils
1000 mils
2000 mils

1.0E+06 1.0E+07 1.0E+08 1.0E+09
Impedance at Port #1
Single 0.01 uF Capacitor at Various Distances (10mil Dielectric)
Cavity Resonance (EZ-PowerPlane) Equivalent Circuit for HSPICE
Impedance Comparison (EZ-PP vs HSPICE) at Port #1
Single 0.01 uF Capacitor at Various Distances (10mil Dielectric)
Current Source Pulse for Simulated IC Power/GND
750 ps Rise/Fall

Time (ns)

Current (amps)
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp) 
Single Capacitor (with 2 nH) at Various Distances (Fullwave Simulation)

-1.5
-1
-0.5
0
0.5
1
1.5
2

0 0.5 1 1.5 2 2.5 3 3.5 4

Time (ns)

Level (volts)

750ps Rise, 35 mil planes, 1uF @ 10mils
750ps Rise, 35 mil planes, 1uF @ 400mils
750ps Rise, 35 mil planes, 1uF @ 800mils
750ps Rise, 35 mil planes, 1uF @ 1200mils
750ps Rise, 35 mil planes, 1uF @ 1600mils
Time Domain Current through Capacitor From Simulated IC Power/GND (1 amp)
Single Capacitor (with 2nH) at Various Distances

- 750ps Rise, 35 mil planes, 1uF @ 10mils
- 750ps Rise, 35 mil planes, 1uF @ 400mils
- 750ps Rise, 35 mil planes, 1uF @ 800mils
- 750ps Rise, 35 mil planes, 1uF @ 1200mils
- 750ps Rise, 35 mil planes, 1uF @ 1600mils
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with No L) at Various Distances

<table>
<thead>
<tr>
<th>Time (ns)</th>
<th>Level (volts)</th>
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<tbody>
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<td>0</td>
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<tr>
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<td>1</td>
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<td>0.0</td>
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<tr>
<td>4</td>
<td>0.0</td>
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</table>

- 750ps Rise, 35 mil planes, 1uF @ 10mils
- 750ps Rise, 35 mil planes, 1uF @ 400mils
- 750ps Rise, 35 mil planes, 1uF @ 800mils
- 750ps Rise, 35 mil planes, 1uF @ 1200mils
- 750ps Rise, 35 mil planes, 1uF @ 1600mils
Time Domain Current through Capacitor From Simulated IC Power/GND (1 amp)
Single Capacitor (with no L) at Various Distances

-750ps Rise, 35 mil planes, 1uF @ 10mils
-750ps Rise, 35 mil planes, 1uF @ 10mils
-750ps Rise, 35 mil planes, 1uF @ 800mils
-750ps Rise, 35 mil planes, 1uF @ 1200mils
-750ps Rise, 35 mil planes, 1uF @ 1600mils
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor with Various Capacitor Connection Inductance

-0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4
0.5
0.6
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5

Level (volts)

Time (ns)

-0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4

750ps Rise, 10 mil planes, 1uF @ 400mils
750ps Rise, 10 mil planes, (2nH) 1uF @ 400mils
750ps Rise, 10 mil planes, (1nH) 1uF @ 400mils
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor with Various Capacitor Connection Inductance

- 1.5
- 1
- 0.5
- 0
- 0.5
- 1
- 1.5

0 0.5 1 1.5 2 2.5 3 3.5 4
Time (ns)

0 0.5 1 1.5 2 2.5 3 3.5 4
Level (volts)

750ps Rise, 10 mil planes, 1uF @ 400mils
750ps Rise, 10 mil planes, (2nH) 1uF @ 400mils
750ps Rise, 35 mil planes, 1uF @ 400mils
750ps Rise, 35 mil planes, (2nH) 1uF @ 400mils
Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin Single Capacitor at Various Distances (Fullwave Simulation)

- 750 ps Rise, 10 mil planes, 1uF, 2 nH
- 750 ps Rise, 10 mil planes, 1uF, 1 nH
- 750 ps Rise, 10 mil planes, 1uF, 0.5 nH
- 750 ps Rise, 10 mil planes, 1uF, No L
Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin
Single Capacitor at Various Distances (Fullwave Simulation)
Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin
Single Capacitor at Various Distances (Fullwave Simulation)

- **750 ps Rise, 35 mil planes, 1uF, 2 nH**
- **750 ps Rise, 35 mil planes, 1uF, 1 nH**
- **750 ps Rise, 35 mil planes, 1uF, 0.5 nH**
- **750 ps Rise, 35 mil planes, 1uF, No L**

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Maximum Time Domain Noise Voltage Across Simulated IC Power/GND Pin Single Capacitor at Various Distances (Fullwave Simulation)

- 1 ns Rise, 35 mil planes, 1uF, 2 nH
- 1 ns Rise, 35 mil planes, 1uF, No L
- 1 ns Rise, 35 mil planes, 1uF, 0.5 nH
- 1 ns Rise, 35 mil planes, 1uF, 1 nH
Maximum Voltage vs Distance to Capacitor for 1 ns Rise/fall time
0.01 uF Capacitor with 0.5 nH ESL and 30 mOhm ESR
So Far……

• Frequency domain simulations not optimum for charge delivery decoupling calculations (phase not considered)
• Time domain simulations using single pulse of current indicate limited capacitor location effect
  – Connection inductance of capacitor much higher than inductance between planes
  – Charge delivered only from the planes
Charge Depletion

- IC draws charge from planes
- Capacitors will re-charge planes
  - Location *does* matter!
Model for Plane Recharge Investigations

Port 2 represents IC current draw

Decoupling Capacitor:
- $C = 1 \mu F$
- $ESR = 30 \text{mOhm}$
- $ESL = 0.5 \text{nH}$

DC voltage used to charge the power plane
Charge Between Planes vs.. Charge Drawn by IC

Board total charge : \[ C \times V = 3.5 \text{nF} \times 3.3 \text{V} = 11 \text{nC} \]

Pulse charge 5A peak : \[ I \times dt / 2 = (1 \text{ns} \times 5 \text{A}) / 2 = 2.5 \text{nC} \]
Triangular pulses (5 Amps Peak)
Noise Voltage from Inductive Effect of Current Draw

Current pulses too small to see charge depletion effects in this time scale
Charge Depletion $\rightarrow$ Voltage Drop

- $L_s = 1 \text{nH}$
- $L_s = 10 \text{nH}$
- $L_s = 50 \text{nH}$

$V_{\text{plane}}$ [V] vs. Time [ns]

- Voltage Drop
- Current [A]
Charge Depletion vs. Capacitor Distance
Charge Depletion for Capacitor @ 400 mils for Various Connection Inductance
Effect of Multiple Capacitors While Keeping Total Capacitance Constant

The decap locations are 800mils, 1200mils, 2700mils from the power pin

- $C=1\mu F$
- $ESL=0.5nH$
- $ESR=1\Omega$

$\varepsilon_r = 4.5$

(power-ground pins at IC center)
Effect of Multiple Capacitors While Keeping Total Capacitance Constant

The decap locations are 800mils, 1200mils, 2700mils from the power pin

(power-ground pins at IC center)

- C=0.5μF
- ESL=0.5nH
- ESR=1Ω

$\varepsilon_r = 4.5$
Effect of Multiple Capacitors While Keeping Total Capacitance Constant

The decap locations are 800mils, 1200mils, 2700mils from the power pin

- \( C = 0.25 \mu F \)
- \( ESL = 0.5nH \)
- \( ESR = 1\Omega \)
Constant Capacitance
800 mil Distance

10 mils thick - V plane

- I input pulses (not in scale)
- 1 decap 800mils
- 2 decap 800mils
- 4 decap 800mils

V_{plane} [V]

3.35

3.3

3.25

3.2

3.15

3.1

0 1 2 3 4 5 6

time [ns]
Constant Capacitance
800 mil Distance

10 mils thick - V plane to 30ns

- I input pulses (not in scale)
- 1 decap 800mils
- 2 decap 800mils
- 4 decap 800mils
Constant Capacitance
1200 mil Distance
Constant Capacitance
1200 mil Distance
Constant Capacitance
2700 mil Distance
Constant Capacitance
2700 mil Distance

![Graph showing the capacitance over time.](image)
Example #1
Low Cap Connection Inductance

IC

Cap

PCB

PWR

GND
Example #2
High Cap Connection Inductance

IC
Cap
PCB

PWR
GND
Example #1
Hi Cap Connection Inductance
Example #1
Lower Cap Connection Inductance
Mutual Inductance Helps Reduce Path Inductance

Do’s

Don’ts

Effect of Capacitor Value??

- Need enough charge to supply need
- Depends on connection inductance

\[ \text{Charge} = C \times V \]
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with No L) with Various Capacitor Values

- 0.4
- 0.3
- 0.2
- 0.1
- 0
- 0.1
- 0.2
- 0.3
- 0.4
- 0.5
- 0.6

750ps Rise, 10 mil planes, (0.0 nH) 1uF @ 400mils
750ps Rise, 10 mil planes, 0.01uF @ 400mils
750ps Rise, 10 mil planes, 100pF @ 400mils

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Dr. Bruce Archambeault
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with 0.5 nH Connection L) with Various Capacitor Values

- 0.4
- 0.3
- 0.2
- 0.1
- 0.0
- 0.1
- 0.2
- 0.3
- 0.4
- 0.5
- 0.6

Level (volts)

0 0.5 1 1.5 2 2.5 3 3.5 4

Time (ns)

- 750ps Rise, 10 mil planes, (0.5nH) 1uF @ 400mils
- 750ps Rise, 10 mil planes, (0.5nH) 0.01 uF @ 400mils
- 750ps Rise, 10 mil planes, (0.5nH) 100 pF @ 400mils
Time Domain Noise Voltage Across Simulated IC Power/GND Pin (1 amp)
Single Capacitor (with 1 nH Connection L) with Various Capacitor Values

-0.4
-0.3
-0.2
-0.1
0
0.1
0.2
0.3
0.4
0.5
0.6
0 0.5 1 1.5 2 2.5 3 3.5 4
Time (ns)

Level (volts)

750ps Rise, 10 mil planes, (1nH) 1uF @ 400mils
750ps Rise, 10 mil planes, (1nH) 0.01uF @ 400mils
750ps Rise, 10 mil planes, (1nH) 1000pF @ 400mils
750ps Rise, 10 mil planes, (1nH) 100pF @ 400mils
Noise Voltage is INDEPENDENT of Amount of Capacitance!

As long as there is ‘enough’ charge

Dist=400 mils
ESR=30mOhms
ESL=0.5nH
Decoupling Summary (1)

• EMC Frequency Domain analysis
  – Steady-state conditions → resonances
  – Transfer function across the board
  – Measurements and simulations agree well
  – Distance of capacitors from ASIC load does not change steady-state impedance
Decoupling Summary (2)

• Charge Delivery Time-Limited analysis
  – Using equivalent SPICE circuit from simulations
  – Current from capacitors change significantly as capacitor moves further away from ASIC
  – Noise at ASIC pins increase significantly as capacitor moves further away from ASIC
  – Steady-state frequency domain analysis not sufficient for charge delivery design of decoupling capacitors
Decoupling Summary (3)

• Recharge the planes
  – Location of Capacitor does matter!
    • Effect more significant for thick dielectrics
  – Connection Inductance is important
  – Value of capacitance not important
  – More capacitors is better than larger/fewer capacitors