IEEE EMC Society Distinguished Lecturer Seminar:
Power Integrity of SiP (System In Package)

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I. Needs of SiP

II. Power Integrity of SiP

III. PDN Design Challenges in SiP

IV. Embedded decoupling capacitor and EBG structures

V. PDN Isolation in SiP design

VI. PDN noise coupling effects on Mixer, LNA, and OpAmp

VI. SSN Free 3D Clock Distribution Network

VIII. Conclusion
Advantages of SiP approach

- Small form factor
- Fast time to market
- Inhomogeneous device integration
- Integration of passive devices, filters, and antenna
- Suitable for RF mobile communication systems
- Low cost
- **Low impedance path** of current-flow at high frequency.
- **Screen out large inductance.**
Simultaneous Switching Noise (SSN):  
\[ \Delta V = L \frac{\Delta I}{\Delta t} \]

- Increase of Maximum Power (Current)
- Increase of Clock Frequency

SSN caused by **simultaneous switching output buffers**
Problems caused by SSN

- Voltage margin reduction
- Logic failure
- Noise coupling to sensitive circuits (RF and analog circuits)
- Circuit reliability degradation (S/N, sensitivity)
- Signal integrity degradation (eye, jitter)
- Electromagnetic radiation
Inductive Impedance of PDN in SiP

\[ L_{\text{total}} = L_{\text{PKG,wire}} + L_{\text{PKG,trace}} + L_{\text{PKG,via}} + L_{\text{PKG,ball}} + L_{\text{PCB,via}} + L_{\text{P/G plane}} + L_{\text{PCB,decap}} \]
Reduction of PDN Inductance

- Locate as close as possible
- Reduce length of interconnect
- Wider, planar interconnect
- Ground/return current path as close as possible, minimal loop size
- Choose low ESL decoupling capacitors
- On chip decap > on-package decap > on-PCB decap
- Thinner PCB and package substrate
- Provide multiple paths (via, pin, wire, decoupling capacitors)
- Choose advanced package

Cost balance needed
Power/Ground Network Impedance

The graph illustrates the comparison between actual and ideal power/ground network impedances across different frequency ranges: kHz, MHz, GHz, THz. The x-axis represents the frequency on a logarithmic scale, while the y-axis represents P/G Impedance. The graph shows that the actual impedance diverges significantly from the ideal impedance at higher frequencies, particularly above the GHz range.

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Frequency Dependent Functions of Discrete Decoupling Capacitor

\[ j\omega L_{VRM} - \frac{j}{\omega C_{VRM}} < \left| j\omega L_{DECAP} - \frac{j}{\omega C_{DECAP}} \right| \]
Frequency Dependent Functions of Discrete Decoupling Capacitor

\[ j \omega L_{DECAP} - \frac{j}{\omega C_{DECAP}} < j \omega L_{VRM} - \frac{j}{\omega C_{VRM}} \]

\[ j \omega L_{DECAP} - \frac{j}{\omega C_{DECAP}} < j \omega L_{PLANE} - \frac{j}{\omega C_{PLANE}} \]

Capacitance given by
Discrete Decoupling Capacitors

Capacitance by
Power/Ground Plane

Inductance by
VRM or
ESL of Bulk Capacitor

Inductance given by
- ESL of Discrete Capacitor
- Mount Pad
- Power/Ground Traces
- Power/Ground Via

Inductance by
Power/Ground Plane

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Good Power Distribution Network

- Battery
- Decoupling Capacitor
- Voltage regulator
- Power plane on PCB
- Package
- Device
- Wire-bond
- Power trace on PCB
Low Impedance Water Pipe

Resistive Pipe

Inductive Pipe
What happens if power distribution network is bad?
What happens if power distribution network is Good?
Advantage and application of PDN analysis in frequency domain

- Intuitive analysis
- Easy to control impedance property

Need for hierarchical PDN simulation

- Interactions between different level PDNs generate high impedance peak.
Case Study: Design of P/G Ring and Bonding Wire for 40Gbps PKG

- The bonding wire length is minimized (1,800 µm → 630 µm), by cutting power/ground rings.

[ Previous Design ]  [ Proposed Design ]
High P/G Plane Impedance made by P/G Plane Resonance

(1,0)/(0,1) : 518MHz

Low Impedance

Mode Suppression

(1,1) : 743MHz

P/G Plane

Center Located

(2,0)/(0,2) : 1043MHz

High Impedance

(2,2) : 1493MHz

\[(f_r)_{mn} = \frac{1}{2\pi\sqrt{\mu_0\varepsilon_r\varepsilon_0}} \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2\]

\[a = b = 14\text{cm}\]
Spectrum Analyzer Measurement of P/G Plane Edge Radiation

TV2 SA Measurement

TV2 P/G Plane Impedance

500 MHz CLK

Edge Radiation (SA-PPG) [dBm]

Frequency [GHz]

1478

3rd

(7cm,7cm)

Short Via
Power/Ground Network Impedance

$20 \log |Z_{PDN}|$

- Parallel circuit resonance
  - $-20 \text{dB/dec lines}$
  - $\omega L_{Total \_Loop1}$
  - $\omega L_{Total \_Loop2}$
  - $\omega L_{Total \_Loop3}$

- Series circuit resonance
  - $20 \text{dB/dec lines}$
  - $C_{\text{decap}1}$
  - $C_{\text{decap}2}$

- Plane cavity resonance modes
  - (1,0)
  - (1/4,0)
  - (1,1)
  - (2,0)

- PKG-level PDN
- Chip-level PDN

Log $f$
Effect of On-chip PDN Design

plane cavity resonance modes

20\log|Z_{PDN}| vs \log f

- On-chip Inductance
- Chip-level PDN
- On-chip decap
- On-chip ESR
On-chip PDN

- Decoupling capacitors using oxide capacitance and MIM capacitance
- Cost sensitive, die size
- ESR considerations needed
- On-chip inductance dominant > 10GHz
- On-chip PDN resonance > 10GHz
- On-chip PDN: direct radiated coupling source
Motivation – Cross-sectional View of Embedded Film Capacitor

1. Removal of SMD Passive Component (Enhanced Routibility)

2. Short Via Length (Low Via Inductance)

3. Small Thickness (Low Inductance)
   High Dielectric Material
   (High Capacitance)
### Fabricated Test Vehicles (with Thin Film Embedded Capacitor)

<table>
<thead>
<tr>
<th>Vehicle Code</th>
<th>Dielectric Thickness</th>
<th>Dielectric Constant (DK)</th>
<th>Capacitance/cm²</th>
<th>Total Capacitance (5cm x 5cm with 2 pairs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>50 μm</td>
<td>4.6</td>
<td>81.46 pF</td>
<td>4.07 nF</td>
</tr>
<tr>
<td>B</td>
<td>25 μm</td>
<td>4.6</td>
<td>162.91 pF</td>
<td>8.15 nF</td>
</tr>
<tr>
<td>C</td>
<td>12 μm</td>
<td>4.6</td>
<td>339.40 pF</td>
<td>16.97 nF</td>
</tr>
<tr>
<td>D</td>
<td>10 μm</td>
<td>16</td>
<td>1416.64 pF</td>
<td>70.83 nF</td>
</tr>
<tr>
<td>E</td>
<td>10 μm</td>
<td>25</td>
<td>2213.50 pF</td>
<td>110.68 nF</td>
</tr>
</tbody>
</table>

**Images:**
- “A” with x50
- “A” with x100
- “A” with x500
- “B” with x500
- “C” with x500
### Measured Impedance Curves (Discrete, Low DK “C”, High DK “E”)

**Power/ground Impedance [dB ohm] vs Frequency [MHz]**

- **16 x 100nF Discrete Capacitors**
  - With Thin Film Embedded Capacitor (Thickness: 12μm, DK: 4.6) – “C”
  - With Thin Film Embedded Capacitor (Thickness: 10μm, DK: 25) – “E”

**Key Observations**:
- **Significant improvement over GHz with Thin Film Embedded Capacitor** *(Very low ESL of Embedded Capacitor)*
- **More improvement at low frequency range with high-DK embedded capacitor** *(More Capacitance)*
High frequency harmonic was amplified with discrete decoupling capacitors (as expected with impedance curve)
Measured SSN (Discrete, Low DK “C”, High DK “E”)

- With Thin Film Embedded Capacitor (Thickness : 12μm, DK : 4.6) – “C”
  - Vp-p : 49.4 mV
  - Low-Frequency Harmonic was appeared with Low DK Embedded Capacitor

- With Thin Film Embedded Capacitor (Thickness : 10μm, DK : 25) – “E”
  - Vp-p : 10.6 mV
  - SSN was almost suppressed with High-DK thin film embedded capacitor
PDN Design Methods

- Frequency dependent capacitance and inductance control
- Increase of decoupling Capacitance depending frequency range (on-chip, on-package, on-PCB, lumped, embedded)
- Decrease of Inductance (line, plane, via, wire, bonds, decoupling capacitors )
- Control resonances (lumped, planar cavity, on-chip, inter-level): avoid overlap with clock and harmonic frequencies
- Control ESR to reduce peak resonance impedance
- Evaluate dc ESR for dc voltage drop estimation
Proposed Modeling Method for Chip-Package-PCB Hierarchical PDN

- Considering all parts in hierarchical PDN and merging them into one using segmentation method.
Analysis of Impedance of Test Vehicle at Package Side

A quite complicated impedance characteristic composed of chip-package-PCB hierarchical PDN is fully analyzed.
Verification of Proposed Modeling Method (Corner on Chip)

- The impedances at corner probe pad on chip
- Frequency: 100MHz to 20GHz
- 5 high impedance peaks
  - 4 peaks → interactions
  - 1 peak → mode resonance of chip
Need for Estimation of High Impedance Peak in Hierarchical PDN

- High impedances in hierarchical PDN from interactions generate problems of system performance degradation.

\[ V_{SSN} = Z_{PDN} \times I_{Circuit} \]

- A precise simulation and analysis of hierarchical PDN is needed.
PDN Noise Coupling Paths in chip and package

- Adjacent interconnections: line, pin, wire
- Via and planes
- Conductive substrates
- Common power line, plane
- Common decoupling capacitors
- Common return current paths
- Isolation techniques needed: Cost, size increase
Waveform and Spectrum of Clock Signal

Graph showing the waveform and spectrum of a clock signal. The waveform is displayed in the first part of the graph, showing the time (ns) on the x-axis and magnitude (mV) on the y-axis. The waveform displays peaks at 5ns and 10ns intervals. The spectrum is shown in the second part of the graph, with frequency (MHz) on the x-axis and power (dBm) on the y-axis. The fundamental frequency is 200MHz, with odd and even harmonics depicted. The graph also includes labels for the fundamental and harmonics.
Spectrum of Wireless Mobile Communication Systems

- AM
- FM
- T-DMB
- TPMS
- GPS
- Wi-Fi
- Bluetooth
- WiBro
- S-DMB
- UWB
- UWB
- RF-ID

 Frequencies:
- AM/FM: 174~216MHz, 535~1,705kHz
- T-DMB: 535~1,705kHz
- TPMS: 433.92MHz
- GPS: 1575.42MHz
- Wi-Fi: 2.4GHz
- Bluetooth: 2.4GHz
- WiBro: 2.3GHz
- S-DMB: 2.6GHz
- UWB: 3.1~4.8GHz
- UWB: 7.2~10.2GHz

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Setup for Analysis

Observation Factors:
1. Transfer Impedance (1,2)
2. Noise Coupling Ratio (1,3)
3. Output Waveform (3)

Pulse Pattern Generator (PPG)
- LO Signal
  - LO Frequency: 915.5MHz
  - LO Voltage: 400mV Pulse

Signal Generator (SG)
- RF Signal
  - Frequency: 915MHz
  - Power: -14dBm
  - Voltage: 60mV Sine Wave

Output Signal
- Frequency: 500kHz
- Power: -2dBm
- Voltage: 250mV
- Voltage Gain: 12dB

DC 2.5V

P/G Noise
- Frequency: 40kHz, 150MHz, 900MHz
- Voltage: 80mV Pulse
Basic Performance of Designed Mixer

- Double Balanced Mixer
- TSMC 0.25um Process
- Target Frequency: 860 ~ 960 MHz
- Gain: 10 ~ 12 dB
- P1dB: -5dBm
- RF Isolation: -30dB
- LO Isolation: -25dB
- Direct Conversion Frequency: 500kHz
On-chip Decap. Effect: Transfer Impedance (Simulation)

- When on-chip decoupling capacitor is designed, transfer impedance decreases more than the case without on-chip decoupling capacitor over 600MHz.

- Transfer impedance decreases when design on-chip decoupling capacitor in 900MHz.
• Switching noise of output waveform with on-chip decoupling capacitor decreases in 13.5dB at a frequency of 900MHz compared to the case without on-chip decoupling capacitor.

-> Verified effect of design on-chip decoupling capacitor in RF or LO frequency band.
When additional off-chip decoupling capacitor is designed, transfer impedance decreases more than the case without additional off-chip decoupling capacitor from 2MHz to 200MHz.

> Transfer impedance decreases when design on-chip decoupling capacitor in 150MHz.
Swicthing noise of output waveform with off-chip decoupling capacitor decreases in 12.2dB a frequency of 150MHz compared to the case without off-chip decoupling capacitor.

-> Verified effect of design off-chip decoupling capacitor in IF frequency band.
Problem by Power and Ground Noise

Digital

DAC

RF & Analog

ADC

Key circuit

Unwanted DC Offset
System Failure!!

Unwanted DC Offset

System Failure!!

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DC Output Offset with Proposed and Conventional Analysis

**DC Output Offset with Proposed Analysis**

![Proposed Analysis Diagram](image)

**DC Output Offset with Conventional Analysis**

![Conventional Analysis Diagram](image)

**Graph:**

- **X-axis:** Frequency (GHz)
- **Y-axis:** DC Output Offset (mV)

**Legend:**
- Conventional analysis
- Proposed analysis

**Text:** Considerable Distinction between DC Output Offset with and without Consideration of PDN
SSN Sensitive Circuits in IC

- VCO: Voltage Controlled Oscillator
- LNA: Low Noise Amplifier
- PLL: Phase Locked Loop
- ADC: Analog to Digital Converter
- DAC: Digital to Analog Converter
SSN Isolation Methods

- Decoupling
- Filtering
- Slot
- Split
- Shielding
- EBG strictures
- Separated power supply/decoupling/return current path
- Separated interconnections: lines, pins, pads, vias
- Separated planes, layers
- Increased separation distance
**PDN Noise Isolation Methods**

**A Chip Level**
- Split On-chip Metal PDN Bus
- Guard Ring (P+/ N+/ Deep-Nwell type)
- On-chip Decoupling Capacitor
- Internal Voltage Regulator

**B Package/PCB Level**
- Split Power/Ground Planes
- On-Package/PCB Decoupling Capacitor (Discrete type, Embedded type)
- Electromagnetic Band Gap (EBG)

→ Frequency dependency of noise isolation
→ Z21 analysis in the frequency domain
The isolation methods of each hierarchical PDN

- By split of PCB and package level PDN, the PDN transfer impedance can be suppressed except around 10MHz.
- By adding on-/off-chip decoupling capacitor, the PDN transfer impedance can be suppressed in both low and high frequency region.
Stack-up for Transceiver SiP [7 layer]

- Thickness = 1.3 mm, Size: 20mmx20mm,
- Ceramic: Dupont (Dielectric Constant = 7.4, Loss Tangent = 0.001)
- Die: 7, Decap: 5개, Ball: 287, Wire-bonding: 53개
- 7 Layers
Transceiver without DS-EBG

-12.17 dBm at 9 GHz

-12.33 dBm at 9 GHz

-43 dBm at 8.999997 GHz

*Power/ Ground noise generates a -43 dBm of unwanted signal* near the output signal.
Transceiver with DS-EBG

- DS-EBG successfully suppresses the unwanted signal by 21 dB.
Proposed On-Interposer EBG Structure

- Capacitive P/G mesh:
  - Width: 80um
  - Space: 120um

- Inductive P/G mesh:
  - Width: 40um
  - Space: 360um
Measurement Results (1/2)

-10 0 21 (dB)

TV A (Mesh)
TV B (EBG)

Mesh PDN
Stopband
Interposer EBG

Coupling Coefficients, S21 (dB)

0 2 4 6 8 10 12 14 16 18 20
Frequency (GHz)

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- Switching noise input at port 1 using 500mVpp clock signal

- Coupled noise spectrum probed at port 2
Proposed 3D Clock Distribution Scheme

3-D Stacked Chip Star-wiring I/O Clock Distribution for Low Jitter, Skew, and Delay

- lossless of bonding-wire & pad
- free from on both on chip and package power supply noise

Clock Distribution Path using Bonding Wire
DLL Output Driver
DLL Replica Path

Stacked Chip
I/O Buffer
DLL Chip
Ball Grid Array Package

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**Enhanced Clock Jitter Performance of the Proposed Scheme**

Conventional On-chip I/O Clock Distribution Scheme

- Peak-to-Peak Jitter: 146 ps
- RMS Jitter: 22 ps

Time [100 ps/div]

Voltage [300 mV/div]

3D Stacked Chip Star-wiring I/O Clock Distribution Scheme

- Peak-to-Peak Jitter: 34 ps
- RMS Jitter: 5 ps

Time [100 ps/div]

Voltage [300 mV/div]

- 3D-stacked chip star-wiring clock scheme provides low clock jitter compared with on-chip clock scheme (77% jitter reduction)

- It is devised to enable the clock signal delivery to be free from on-chip digital switching noise and package power/ground cavity noise coupling.
Advantages of Proposed PCR CDN for 3D Stacked Chip Package

- Jitter is filtered by high-Q bandpass filter utilizing a package level quarter-wavelength planar cavity resonator
- Reduction of the number of cascaded repeaters
• Uniform phase and uniform amplitude standing wave is used for clock distribution
Quarter-wavelength Resonator with Inductive Termination

- Voltage at $\lambda/2$
- Voltage at $\lambda/4$

Incident wave

Inductive Termination

Open

Short
Measure Eyd-diagram of PCR CDN with Noise

Clock source before distribution

- Pk-to-pk jitter = 98 ps
- Eye-opening = 920 mV

Distributed clock at planar cavity resonator output

- Pk-to-pk jitter = 28 ps
- Eye-opening = 1720 mV

<table>
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<th>Distributed clock</th>
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<td>28 ps</td>
</tr>
<tr>
<td>Eye-opening</td>
<td>920 mV</td>
<td>1720 mV</td>
</tr>
</tbody>
</table>

- Clock frequency : 1.55 GHz
- Clock magnitude : 1 Vp-p
- Switching noise : 300 mV
Unique Research Focus

High-performance Mixed Mode System

- System on Chip (On-Chip Level)
- System in Package (On-Package Level)
- Module, PCB, Cabling (System Level)

Co-Design

Signal Integrity
- Low Noise and High-Integration Design

Power Integrity

Electromagnetic Interference

Improvement of Reliability, Performance, Design Cycle, Cost
Conclusion

- Significant noise coupling occurs from digital PDN to noise sensitive RF and analog circuits on a same SiP.
- The clock frequencies and harmonic frequencies should be placed away from the RF carrier frequencies.
- Low PDN impedance should be maintained.
- PDN resonance frequencies should be placed away not only from the clock frequencies, and their harmonic frequencies, but also from RF carrier frequencies.
- Via and wire are a major noise coupling path from digital PDN to noise sensitive circuits.
- Noise coupling reduction methods including using PDN design, frequency control, filtering, separation/isolation, decoupling, shielding, and grounding techniques.
- Case studies: LNA, Clock distribution network
- Chip-package co-design can provide optimal and cost-effective solutions.