IEEE EMC Society Distinguished Lecturer Seminar:

Power Integrity of SiP (System In Package)

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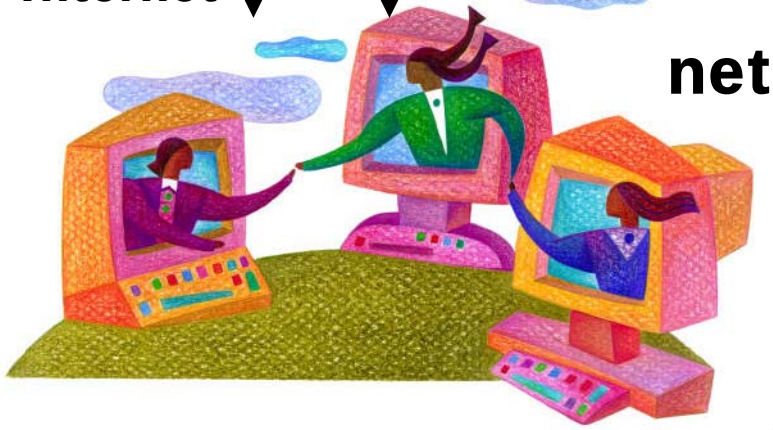
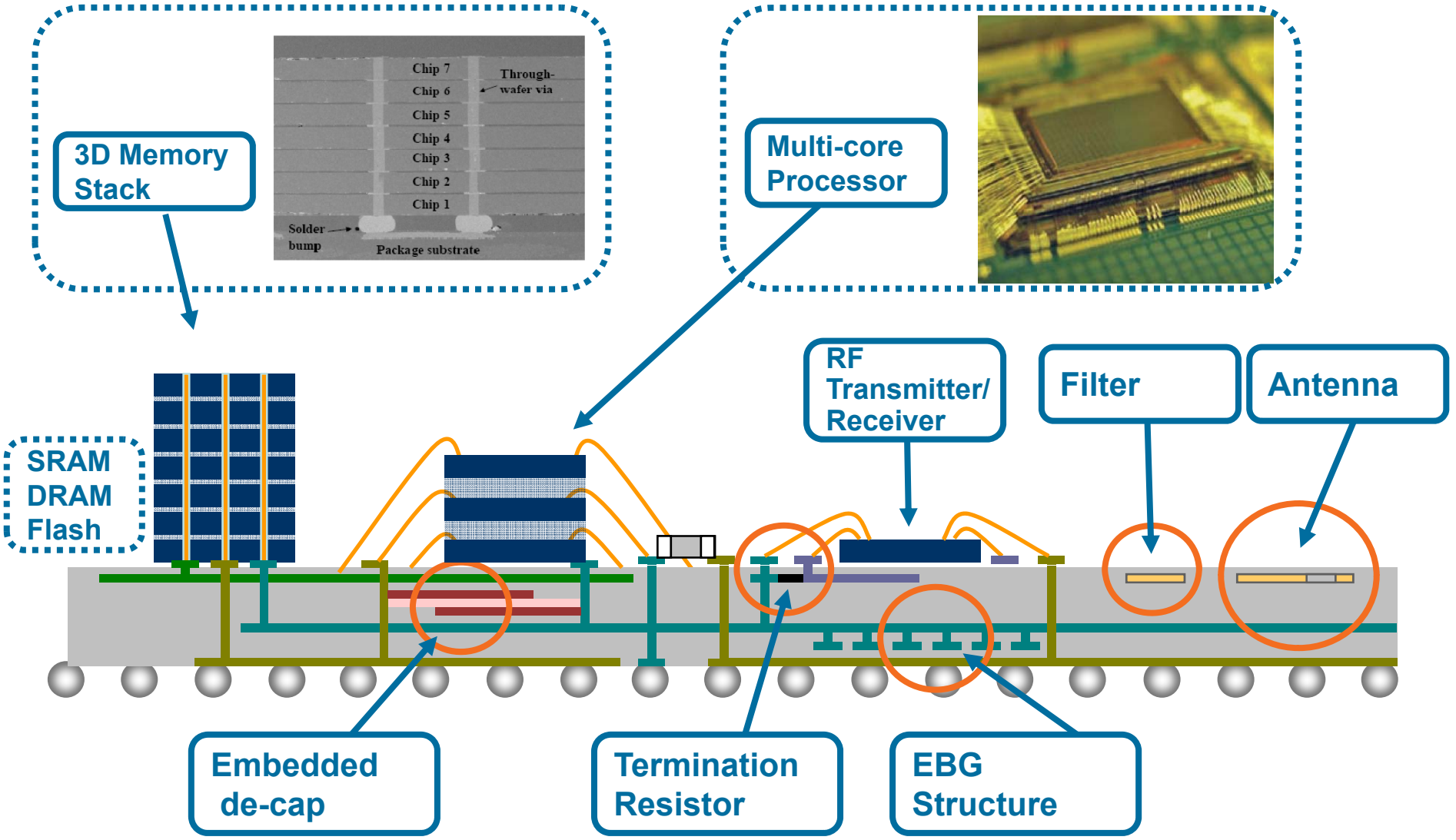


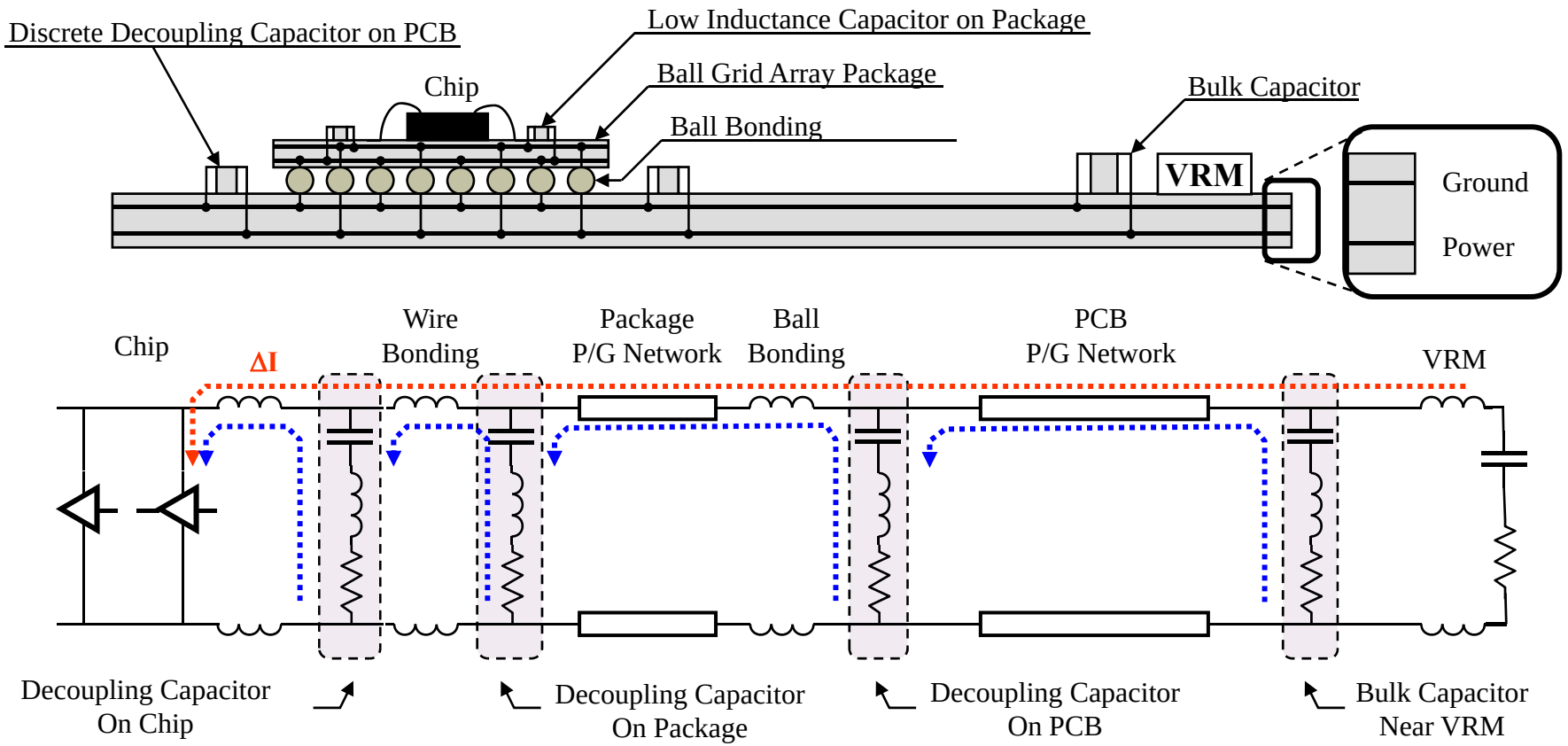
3D Convergence System In Package



Advantages of SiP approach

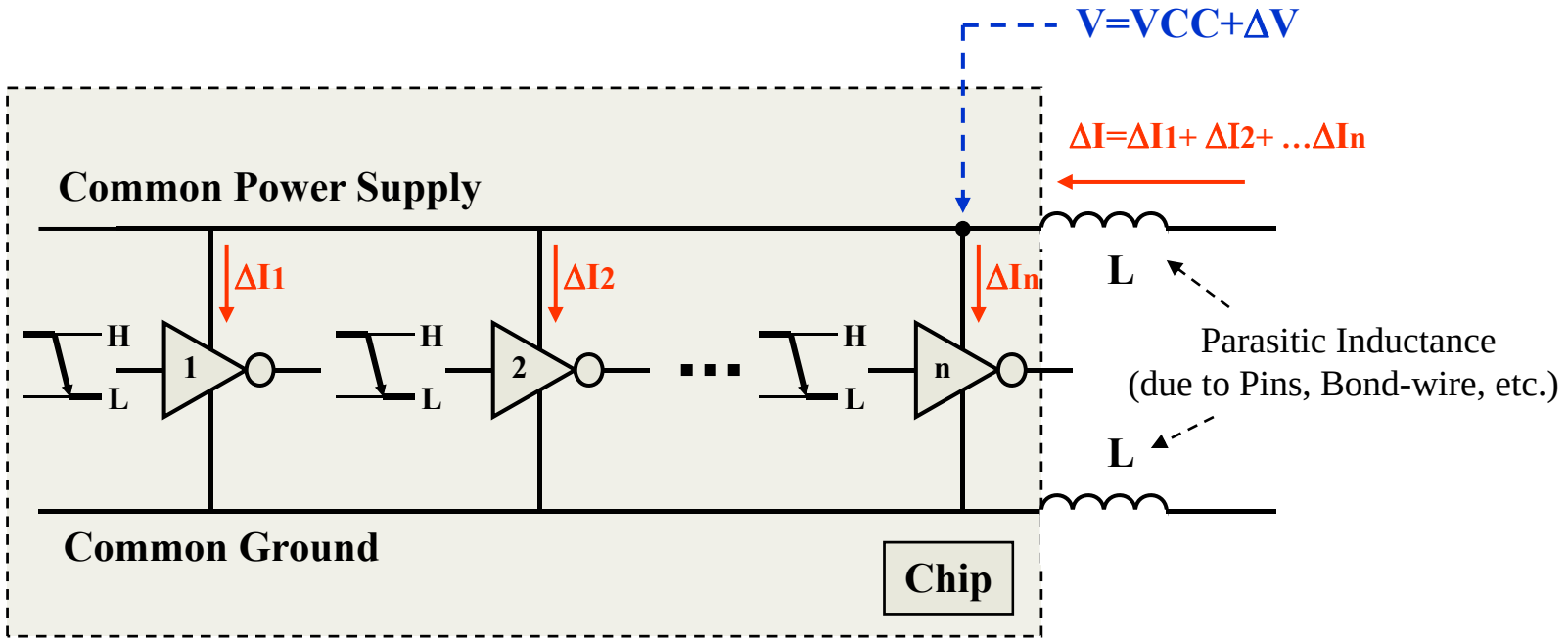
- Small form factor
- Fast time to market
- Inhomogeneous device integration
- Integration of passive devices, filters, and antenna
- Suitable for RF mobile communication systems
- Low cost

Power Supply Current Path



- **Low impedance path of current-flow at high frequency.**
- **Screen out large inductance.**

Simultaneous Switching Noise (SSN)



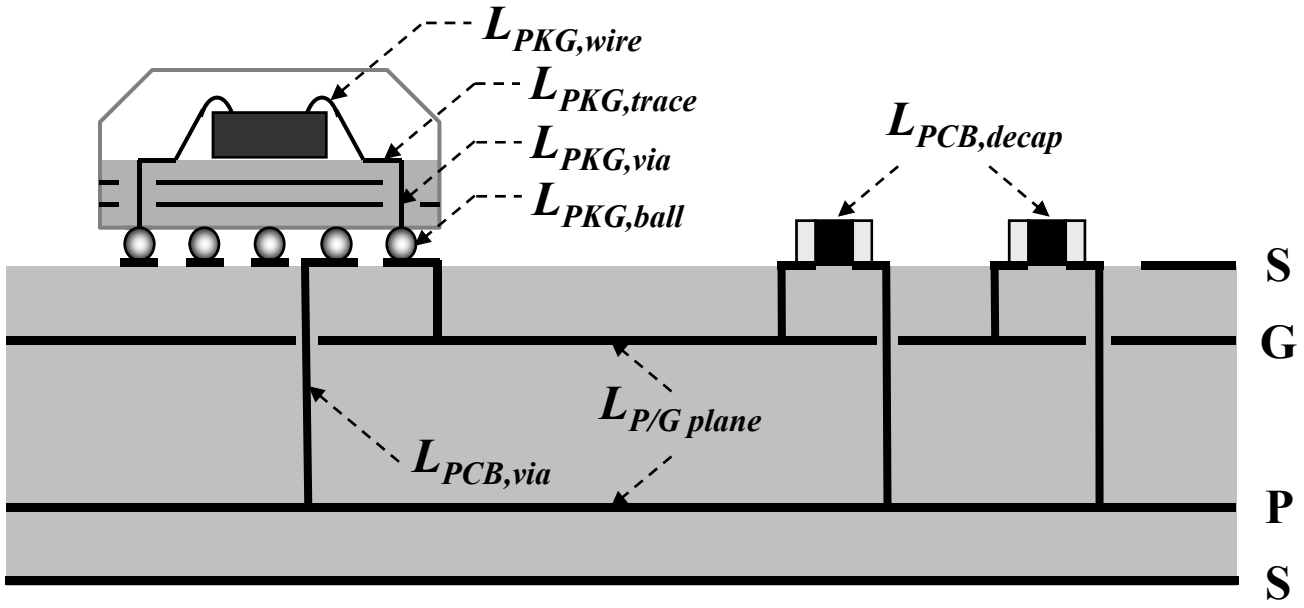
- **Simultaneous Switching Noise (SSN) :** $\Delta V = L \frac{\Delta I}{\Delta t}$
  - Increase of Maximum Power (Current)
  - Increase of Clock Frequency

- **SSN caused by simultaneous switching output buffers**

Problems caused by SSN

- Voltage margin reduction
- Logic failure
- Noise coupling to sensitive circuits (RF and analog circuits)
- Circuit reliability degradation (S/N, sensitivity)
- Signal integrity degradation (eye, jitter)
- Electromagnetic radiation

Inductive Impedance of PDN in SiP

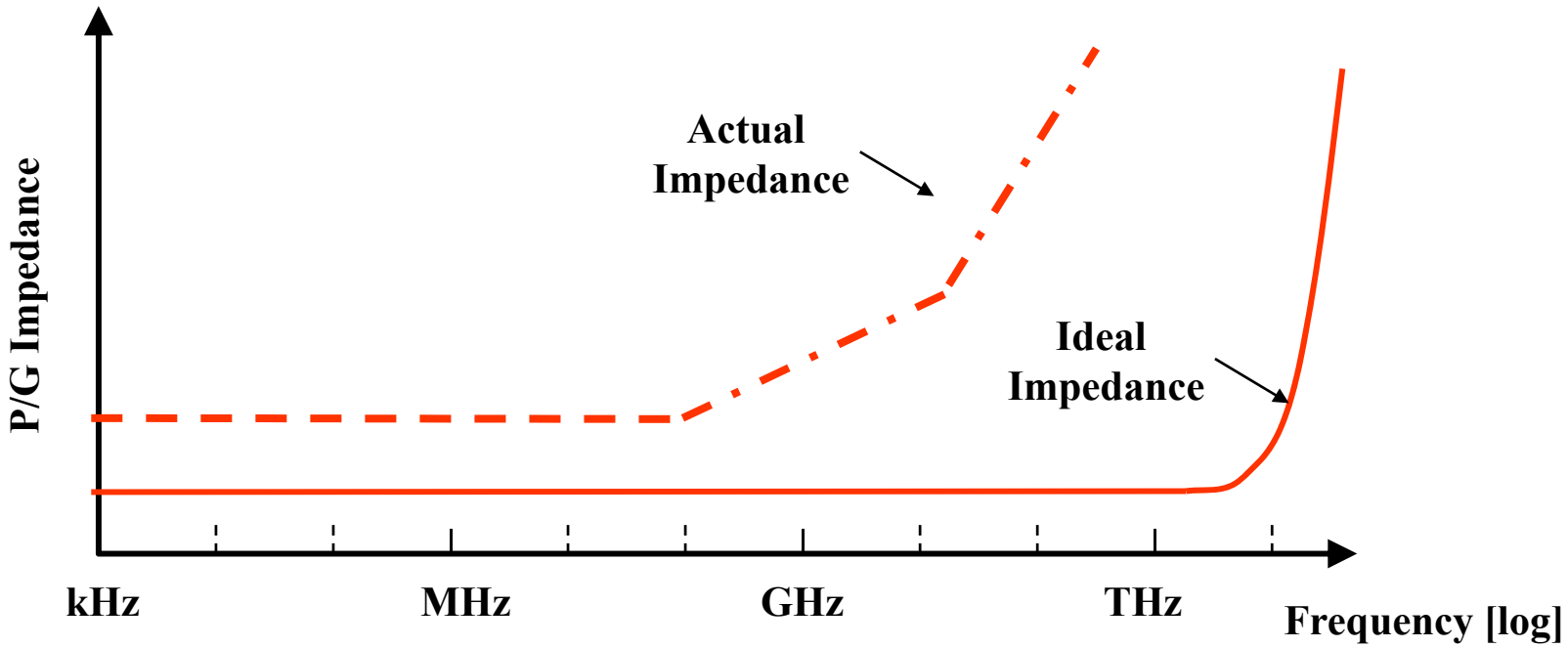


$$L_{totlal} = L_{PKG,wire} + L_{PKG,trace} + L_{PKG,via} + L_{PKG,ball} + L_{PCB,via} + L_{P/G\ plane} + L_{PCB,decap}$$

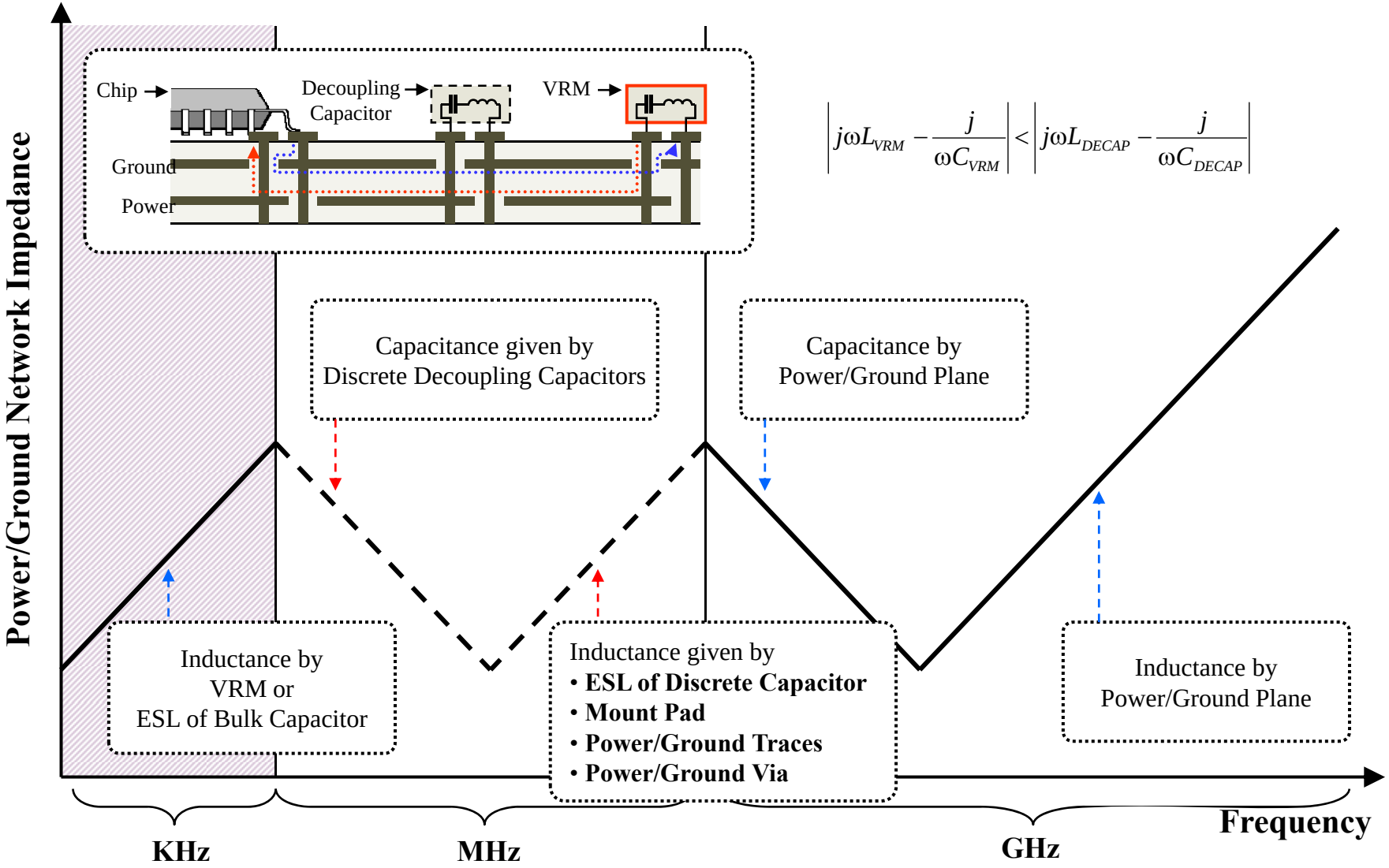
Reduction of PDN Inductance

- Locate as close as possible
- Reduce length of interconnect
- Wider, planar interconnect
- Ground/return current path as close as possible, minimal loop size
- Choose low ESL decoupling capacitors
- On chip decap > on-package decap > on-PCB decap
- Thinner PCB and package substrate
- Provide multiple paths (via, pin, wire, decoupling capacitors)
- Choose advanced package
- Cost balance needed

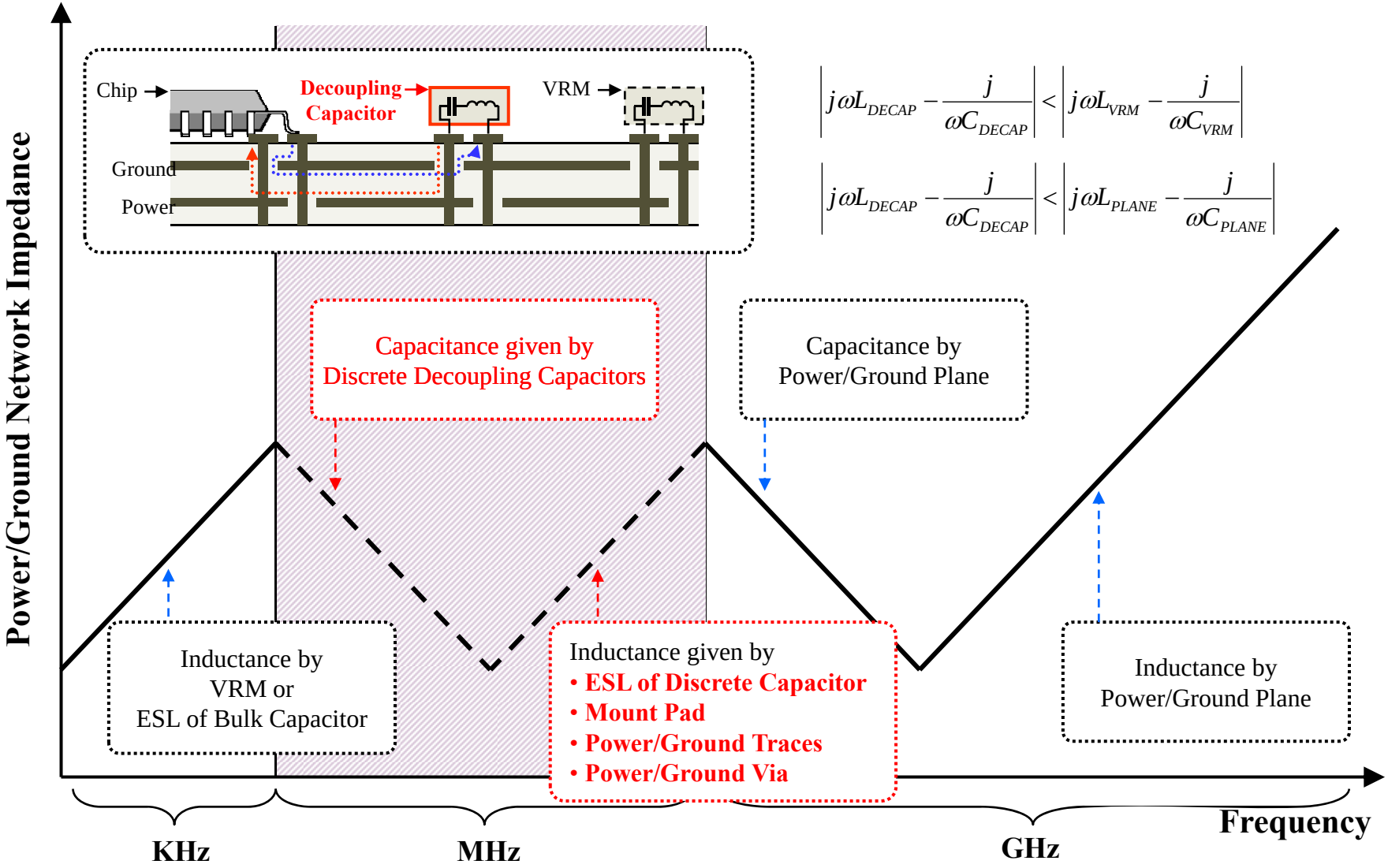
Power/Ground Network Impedance



Frequency Dependent Functions of Discrete Decoupling Capacitor



Frequency Dependent Functions of Discrete Decoupling Capacitor



Good Power Distribution Network

Decoupling Capacitor

Power plane on PCB

Voltage regulator

Package

Device

Wire-bond

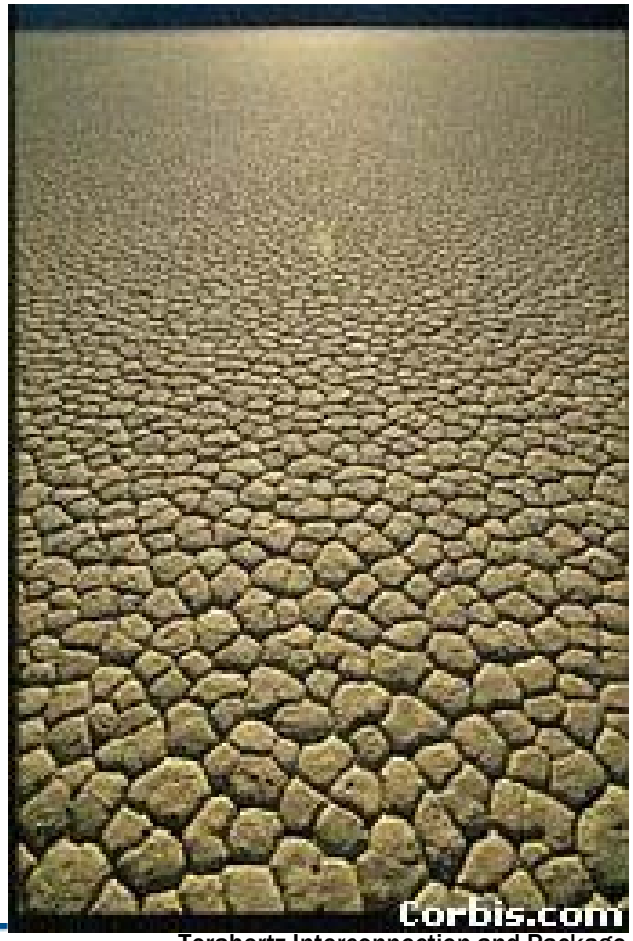
Power trace on PCB

Low Impedance Water Pipe

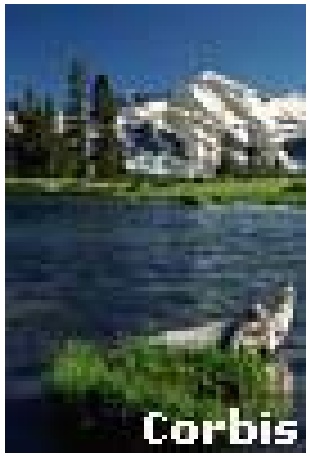
Resistive Pipe

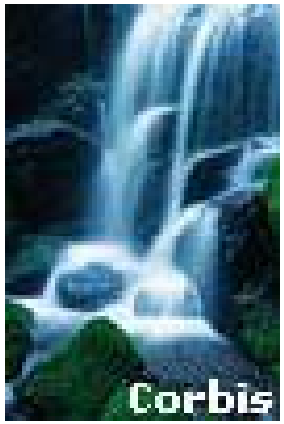
Inductive Pipe

What happens if power distribution network is bad?

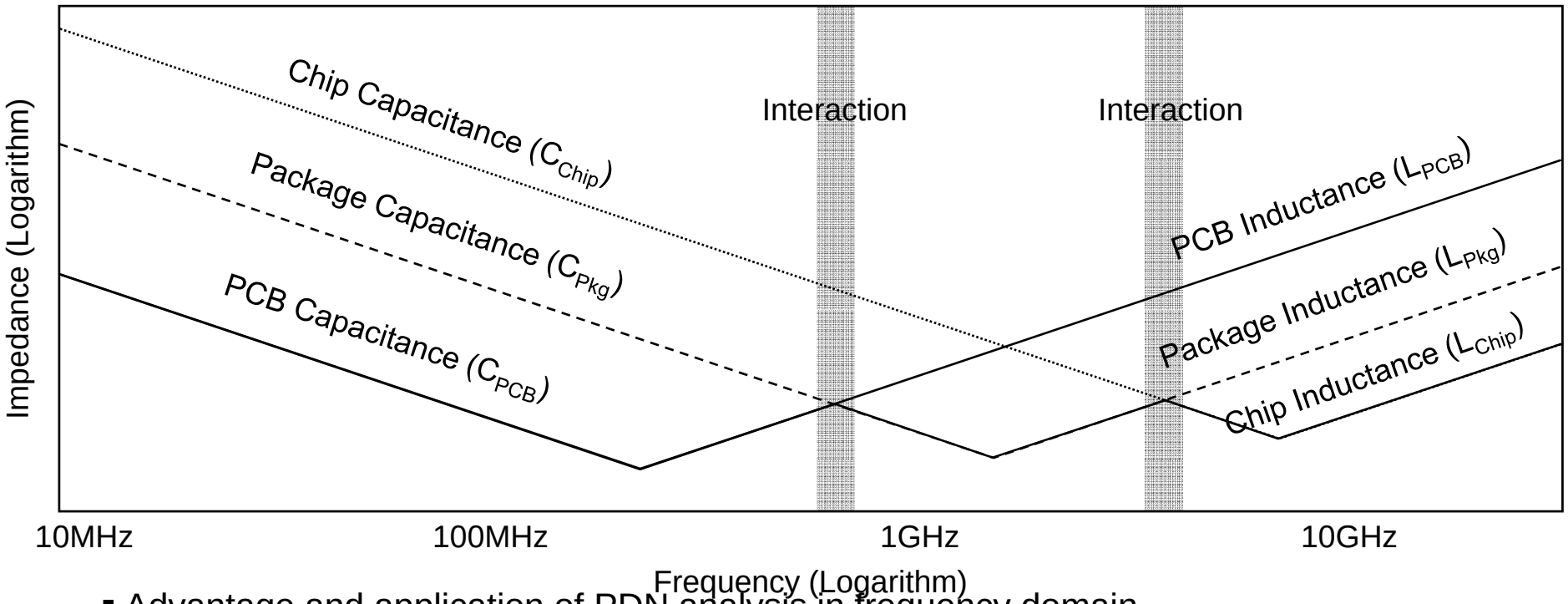


What happens if power distribution network is Good?





Impedance Property of Chip-Package-PCB Hierarchical PDN



- Advantage and application of PDN analysis in frequency domain

- Intuitive analysis

- Easy to control impedance property

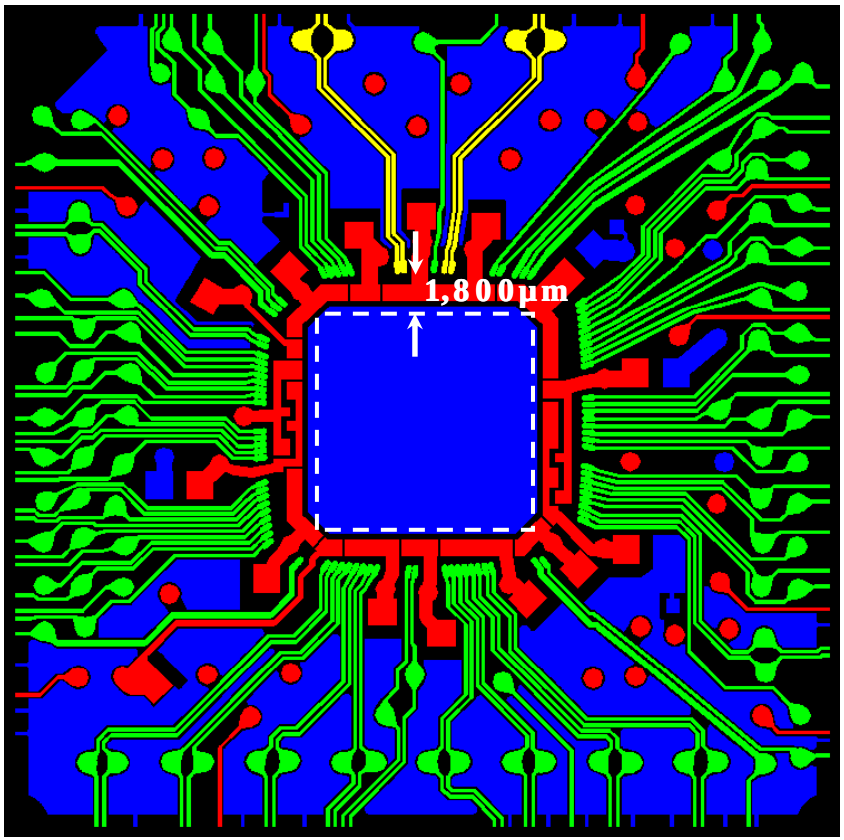
- Need for hierarchical PDN simulation

- Interactions between different level PDNs generate high impedance peak.

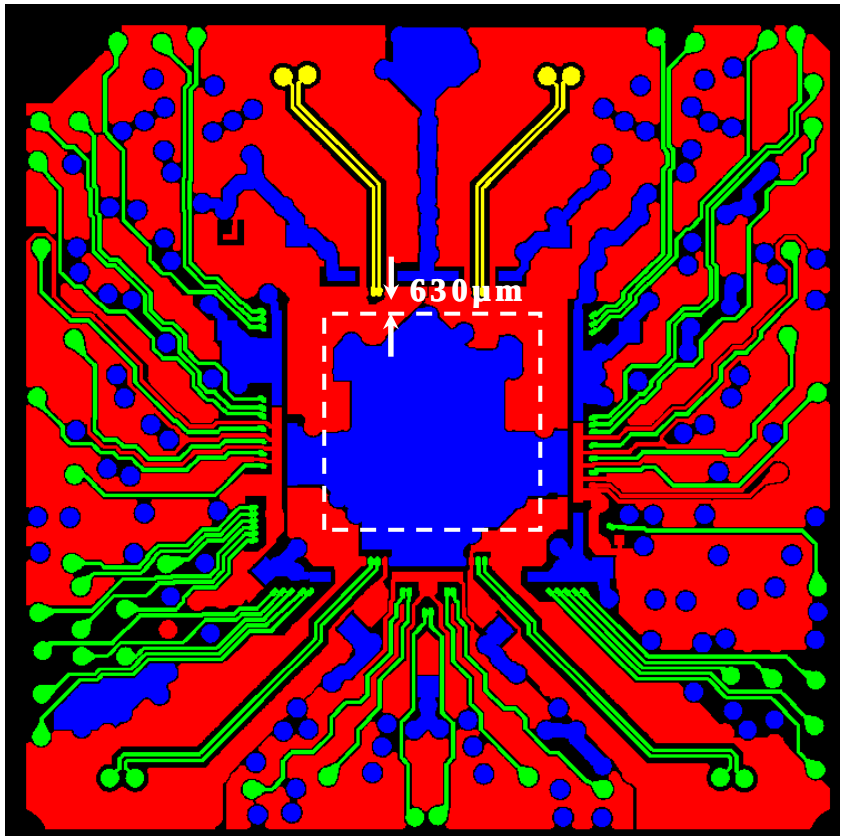
Case Study : Design of P/G Ring and Bonding Wire for 40Gbps PKG

- The bonding wire length is minimized (1,800 μm → 630 μm), by cutting power/ground rings.

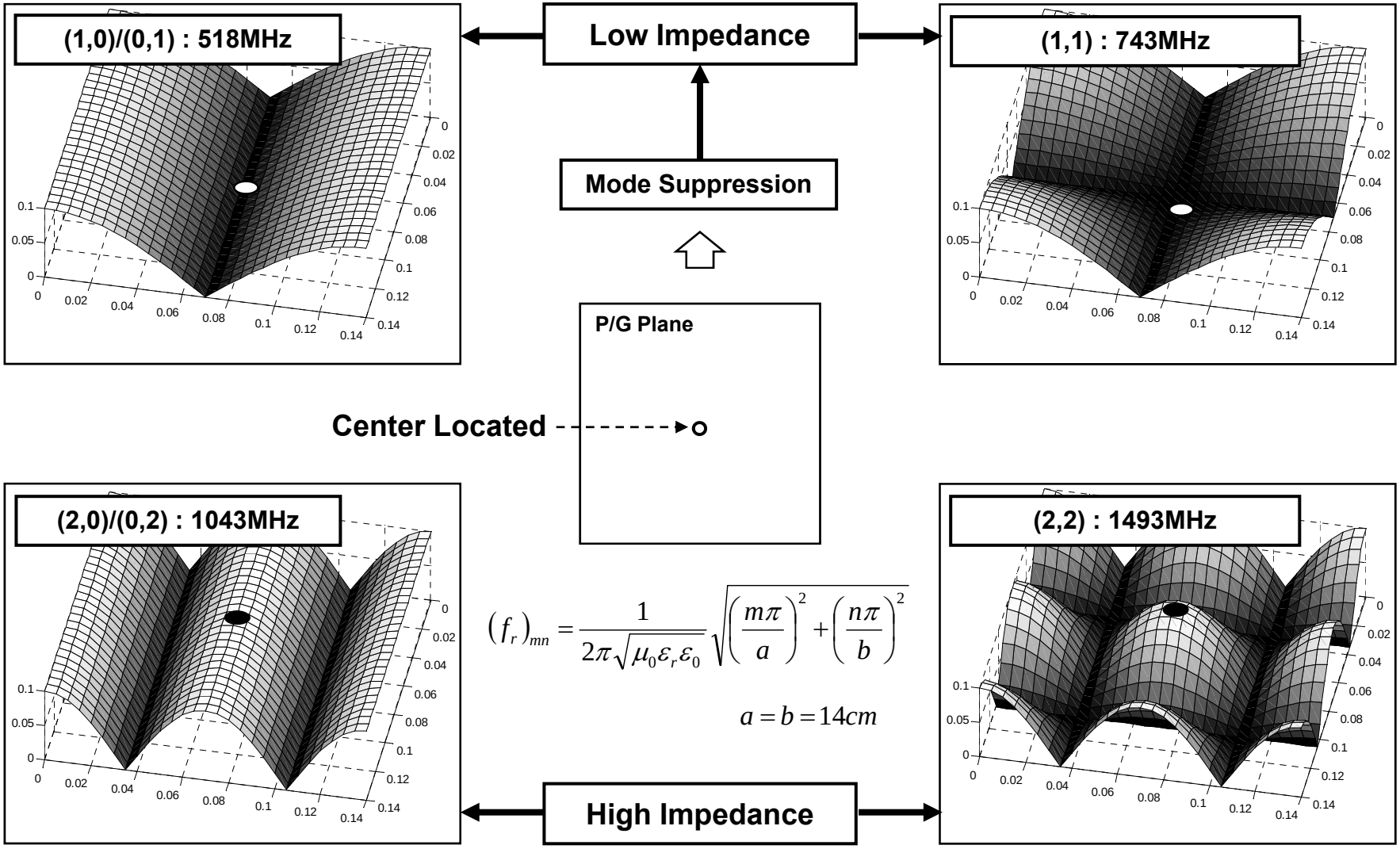
[Previous Design]



[Proposed Design]



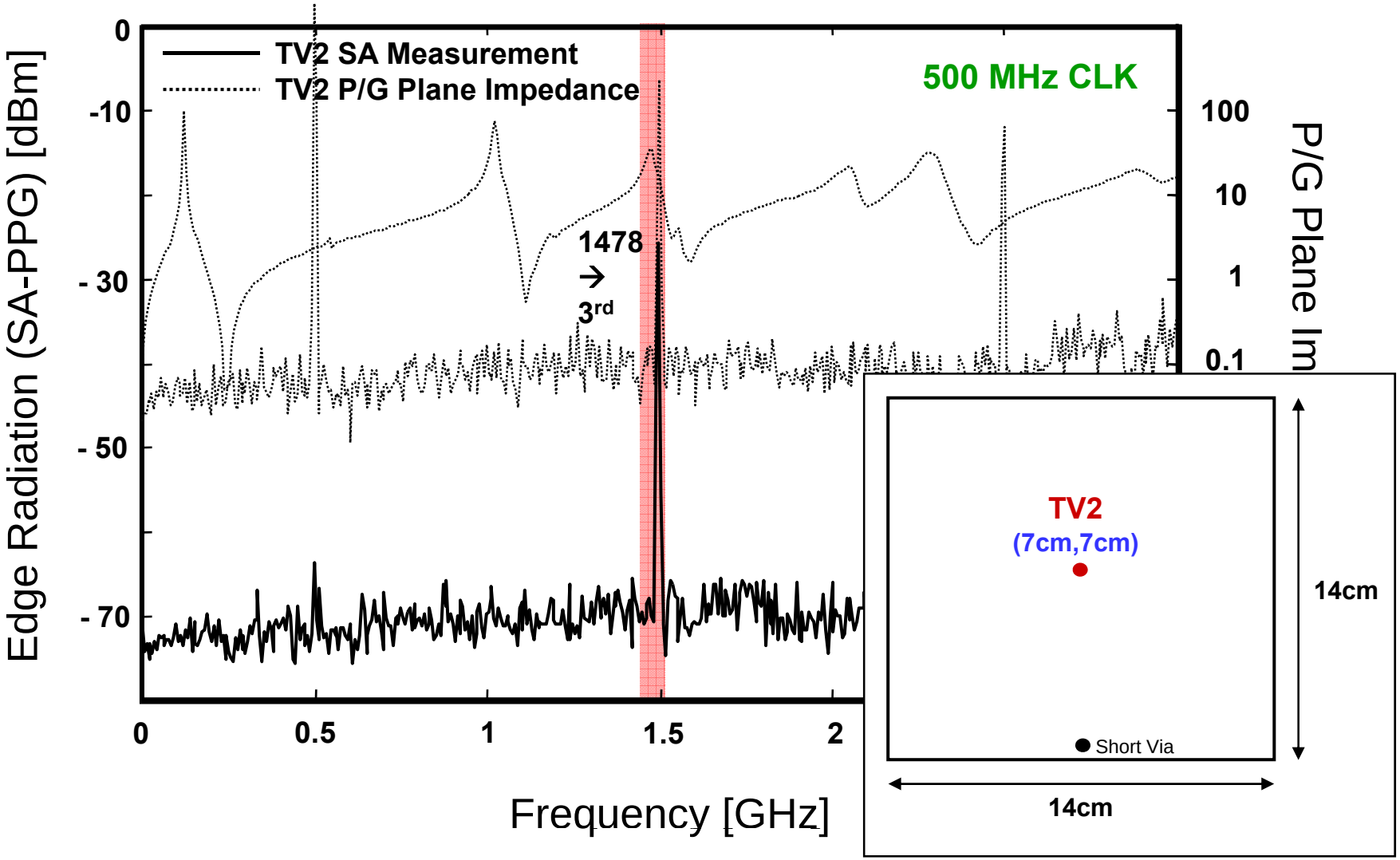
High P/G Plane Impedance made by P/G Plane Resonance



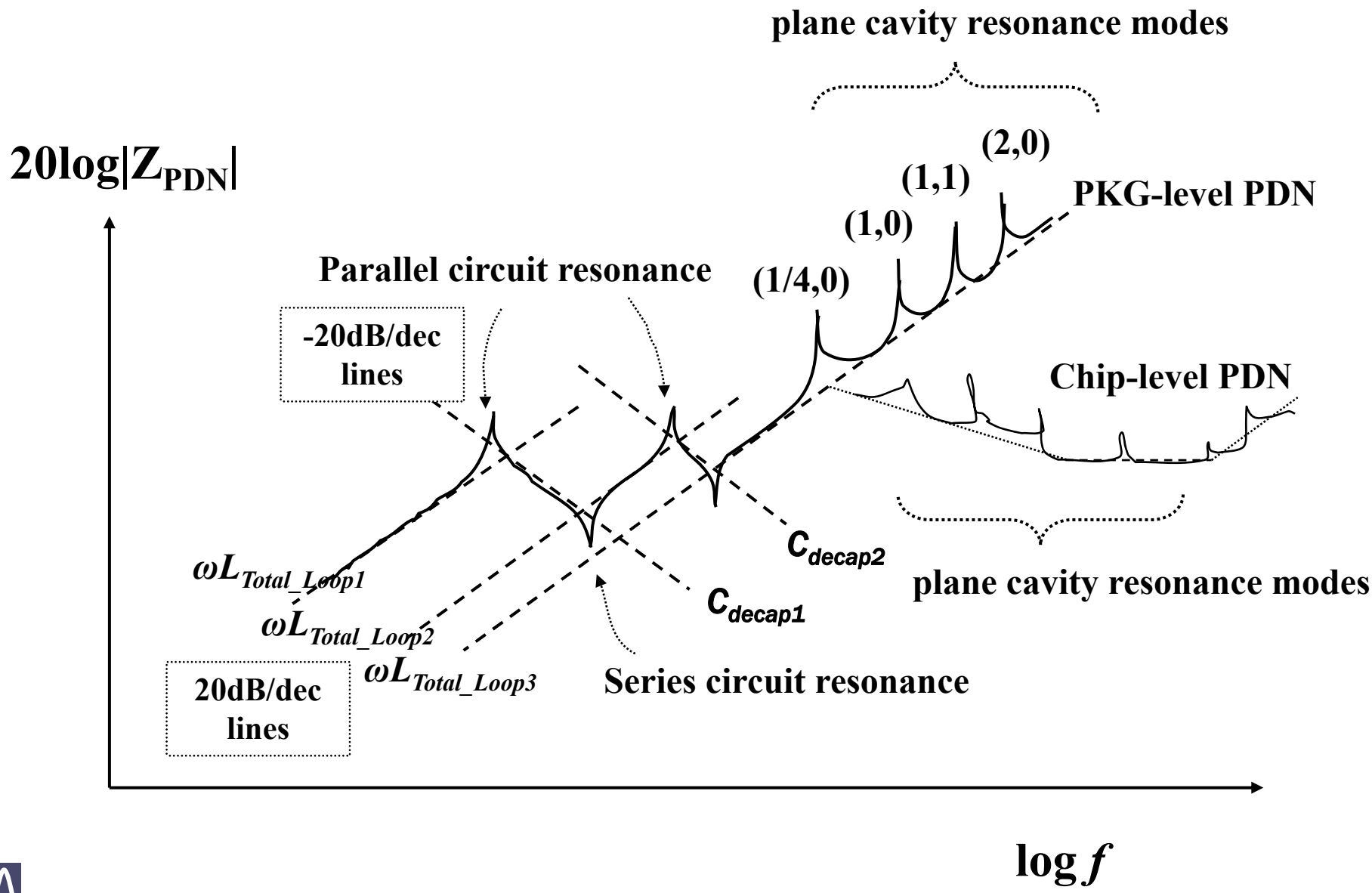
$$(f_r)_{mn} = \frac{1}{2\pi\sqrt{\mu_0 \varepsilon_r \varepsilon_0}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}$$

$$a = b = 14cm$$

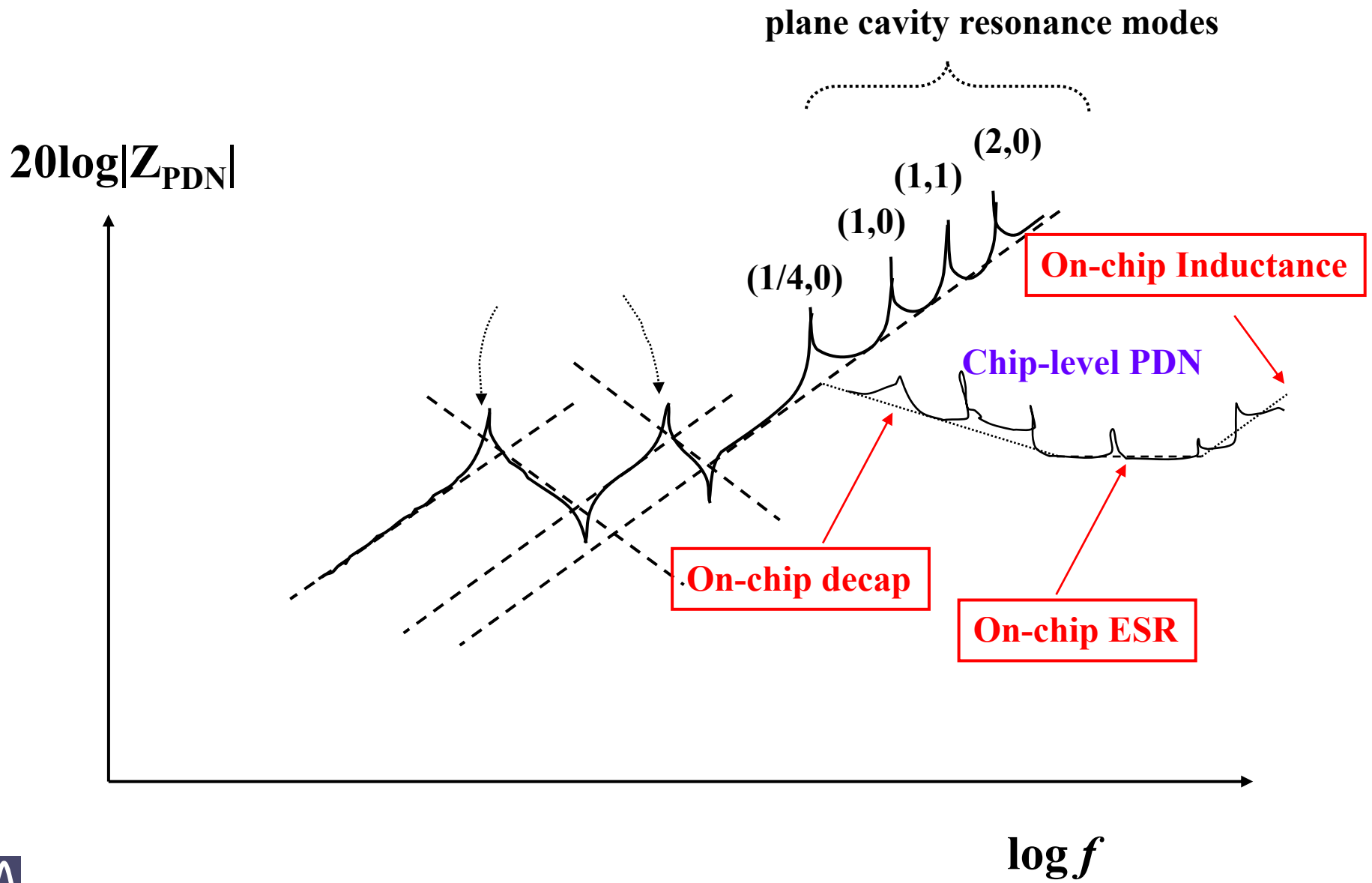
Spectrum Analyzer Measurement of P/G Plane Edge Radiation



Power/Ground Network Impedance



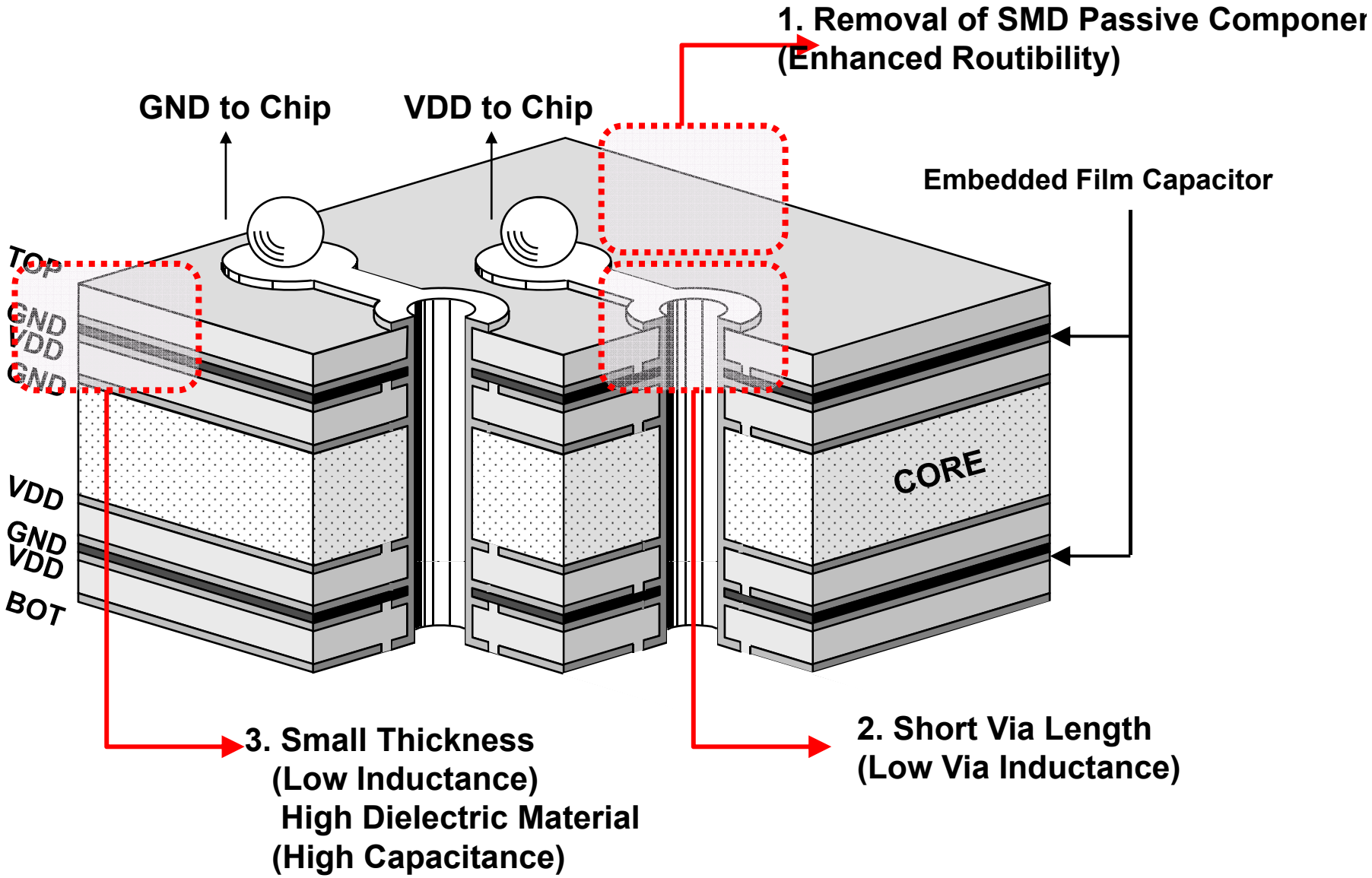
Effect of On-chip PDN Design



On-chip PDN

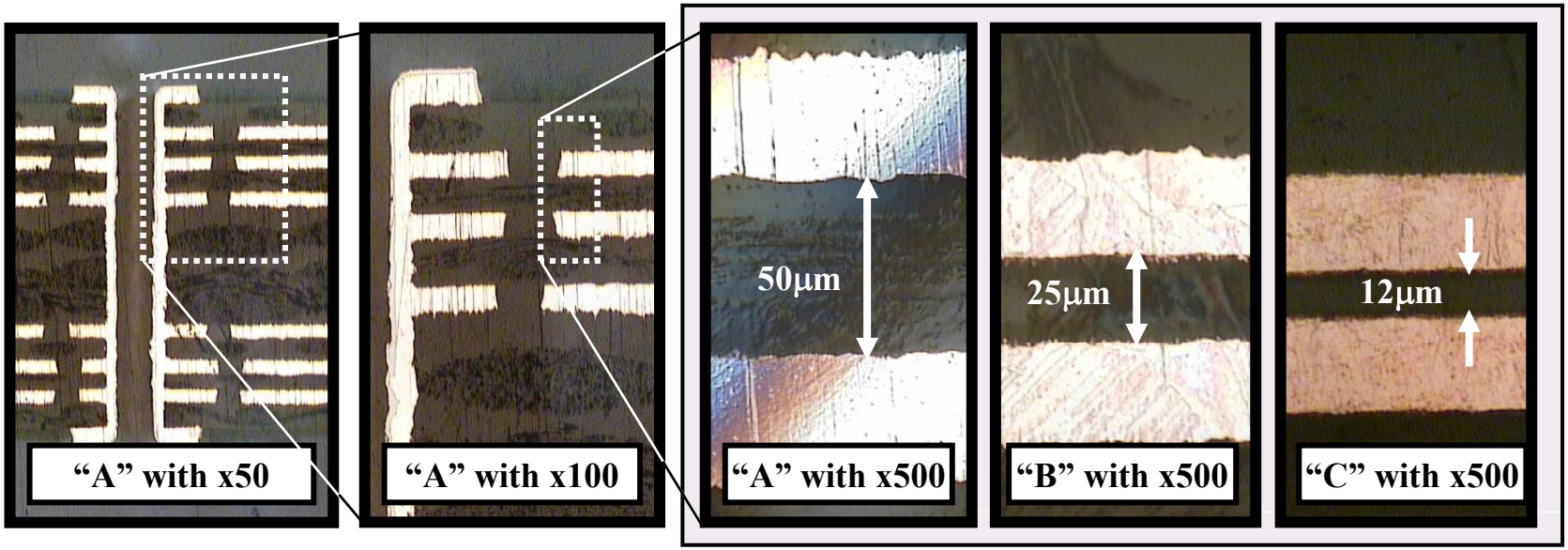
- Decoupling capacitors using oxide capacitance and MIM capacitance
- Cost sensitive, die size
- ESR considerations needed
- On-chip inductance dominant > 10GHz
- On-chip PDN resonance > 10GHz
- On-chip PDN: direct radiated coupling source

Motivation –Cross-sectional View of Embedded Film Capacitor

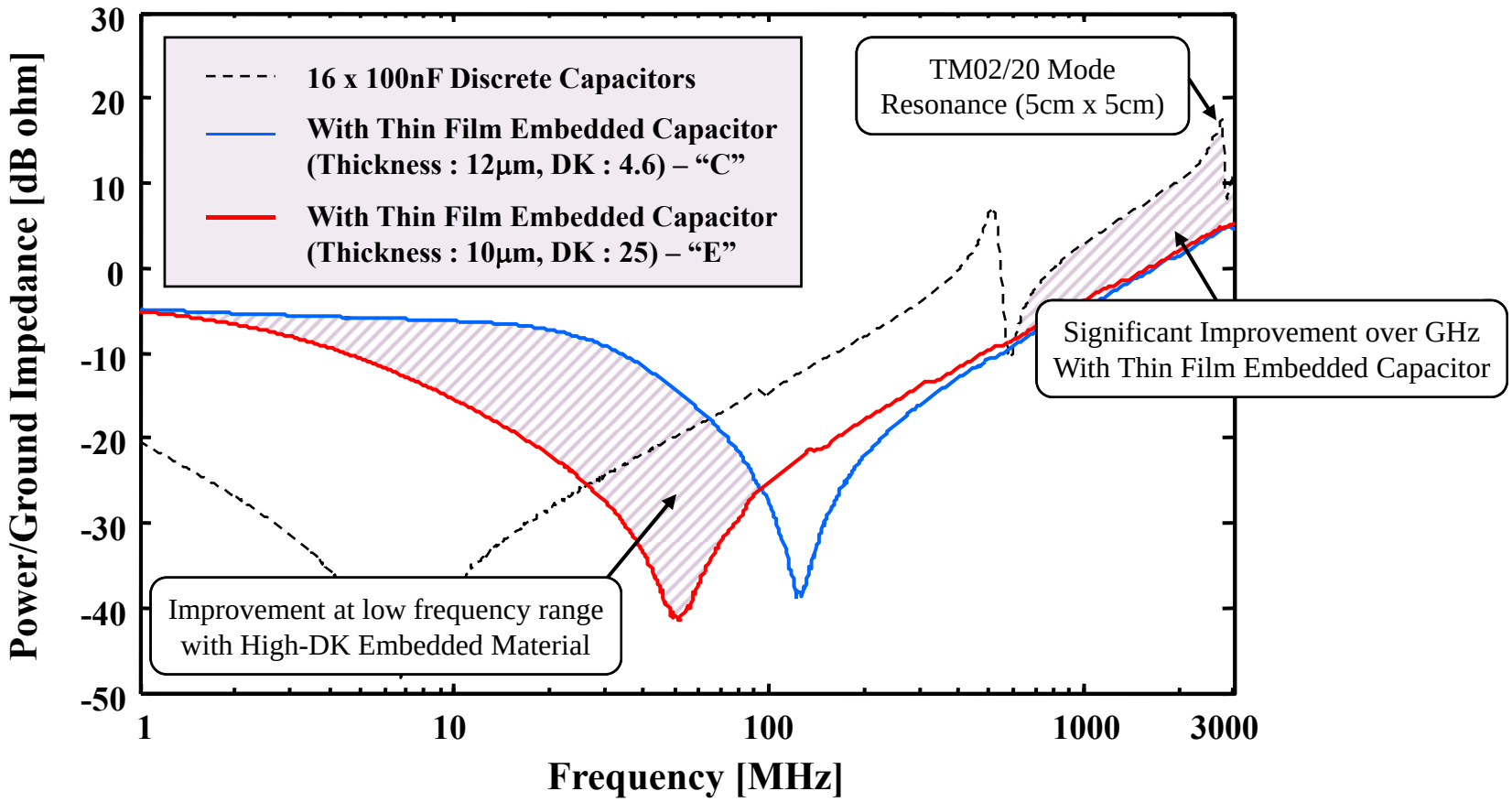


Fabricated Test Vehicles (with Thin Film Embedded Capacitor)

Vehicle Code	Dielectric Thickness	Dielectric Constant (DK)	Capacitance/cm²	Total Capacitance (5cm x 5cm with 2 pairs)
A	50 μm	4.6	81.46 pF	4.07 nF
B	25 μm	4.6	162.91 pF	8.15 nF
C	12 μm	4.6	339.40 pF	16.97 nF
D	10 μm	16	1416.64 pF	70.83 nF
E	10 μm	25	2213.50 pF	110.68 nF

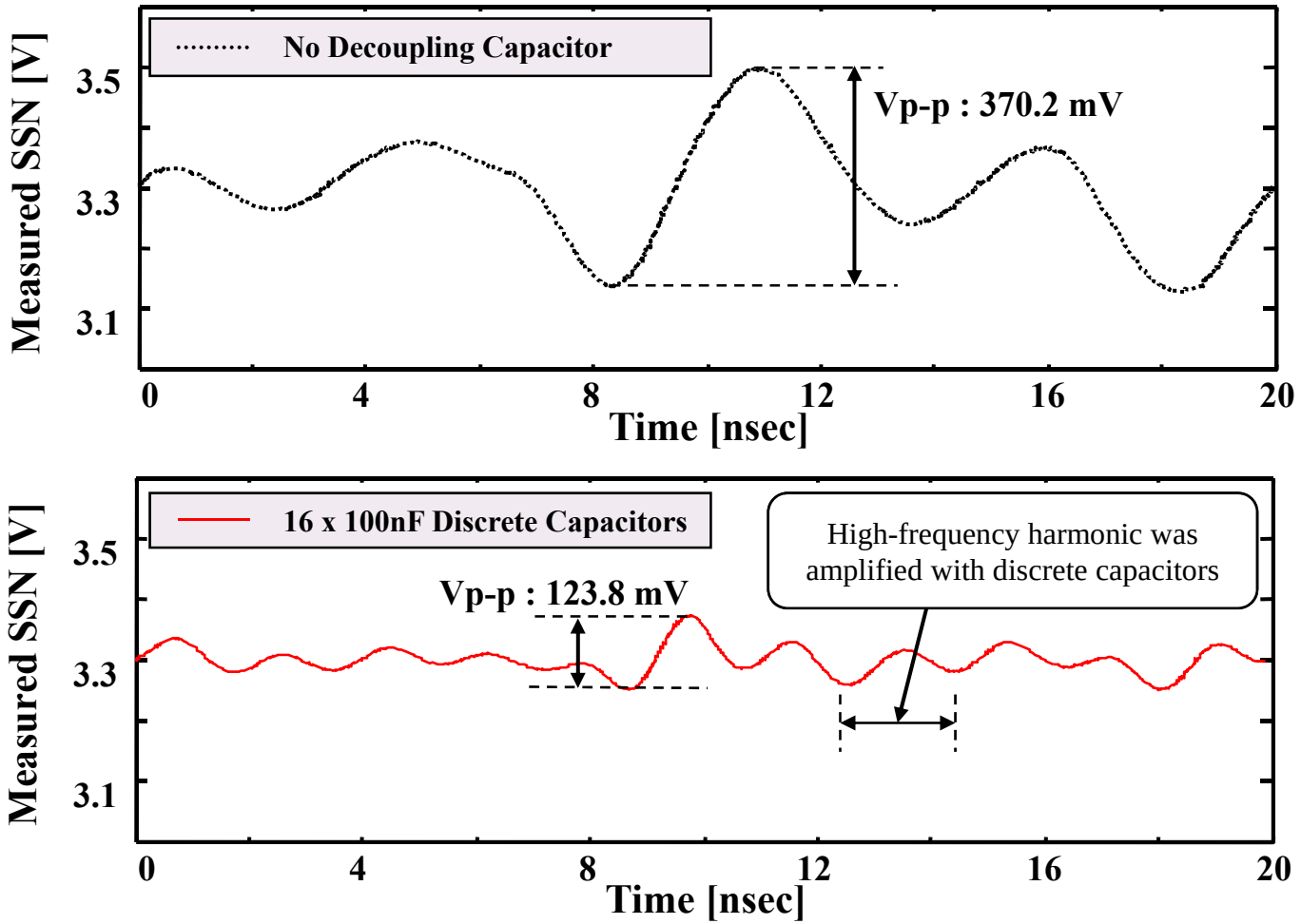


Measured Impedance Curves (Discrete, Low DK "C" , High DK "E")



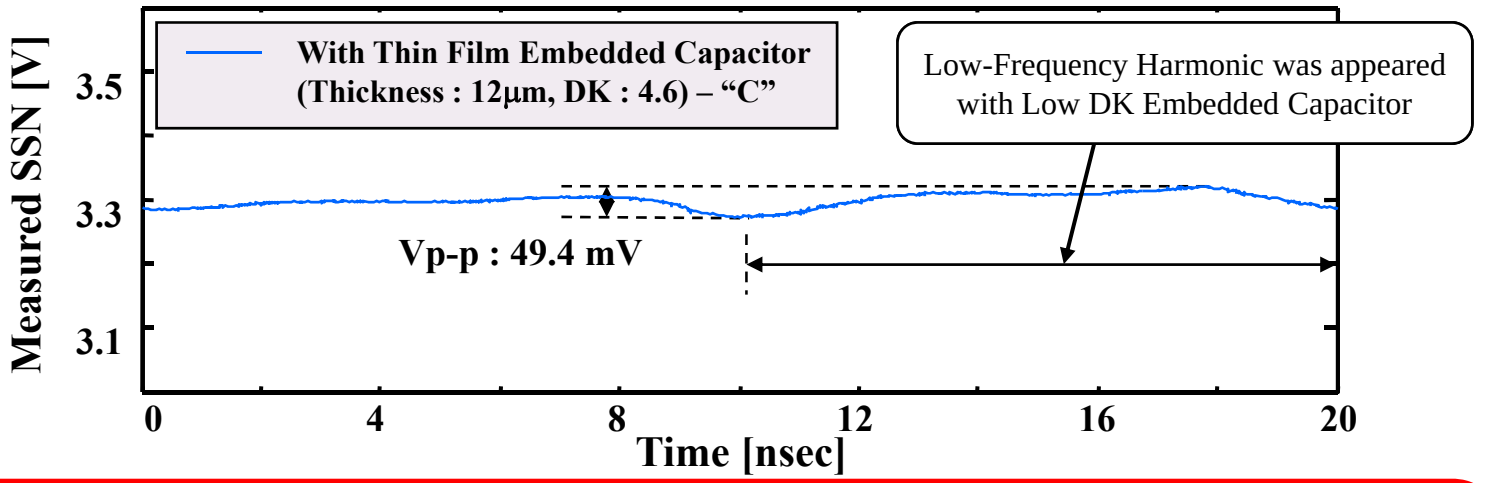
- Significant improvement over GHz with Thin Film Embedded Capacitor (**Very low ESL of Embedded Capacitor**)
- More improvement at low frequency range with high-DK embedded capacitor (**More Capacitance**)

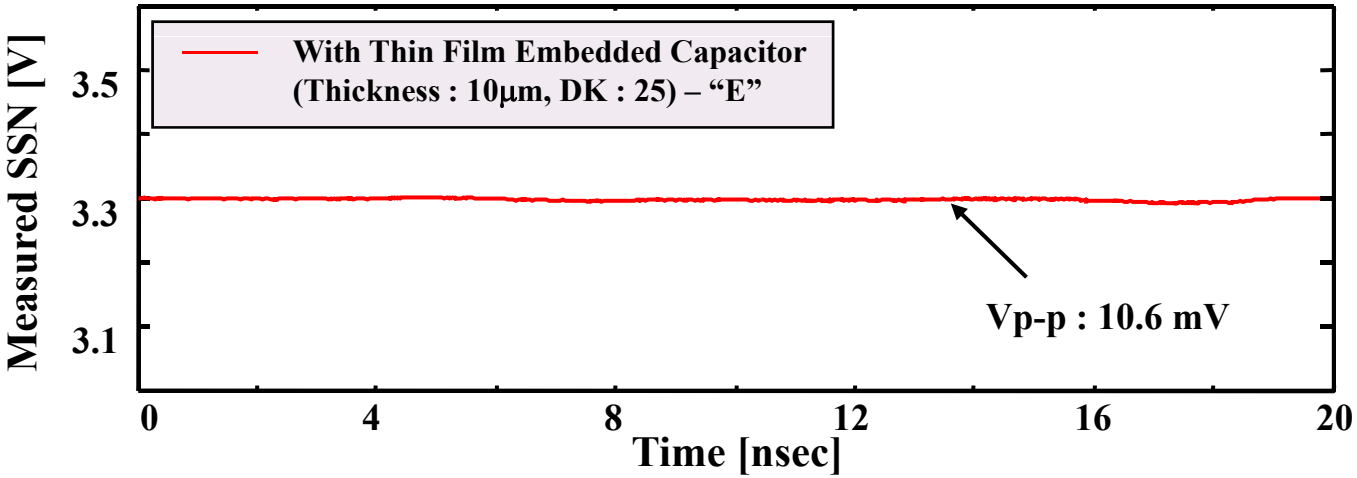
Measured SSN (No De-Cap. Vs. Discrete De-Cap.)



- High frequency harmonic was amplified with discrete decoupling capacitors (as expected with impedance curve)

Measured SSN (Discrete, Low DK "C" , High DK "E")



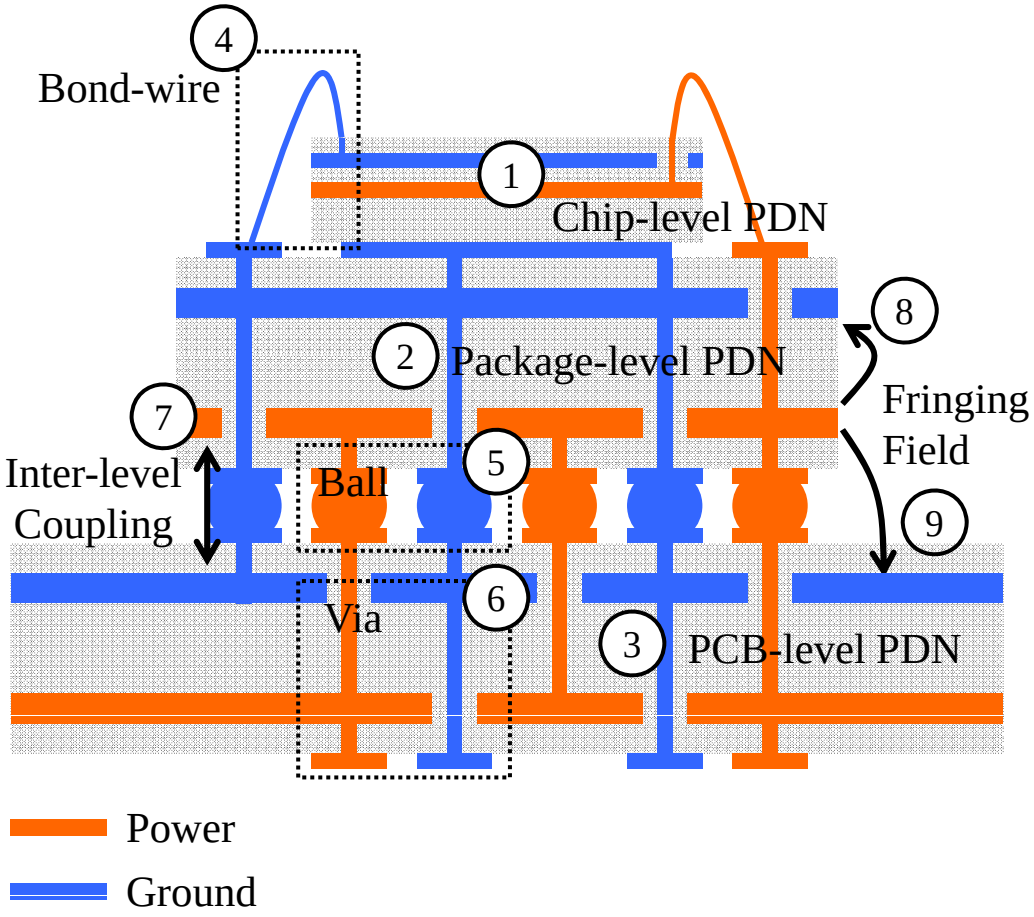


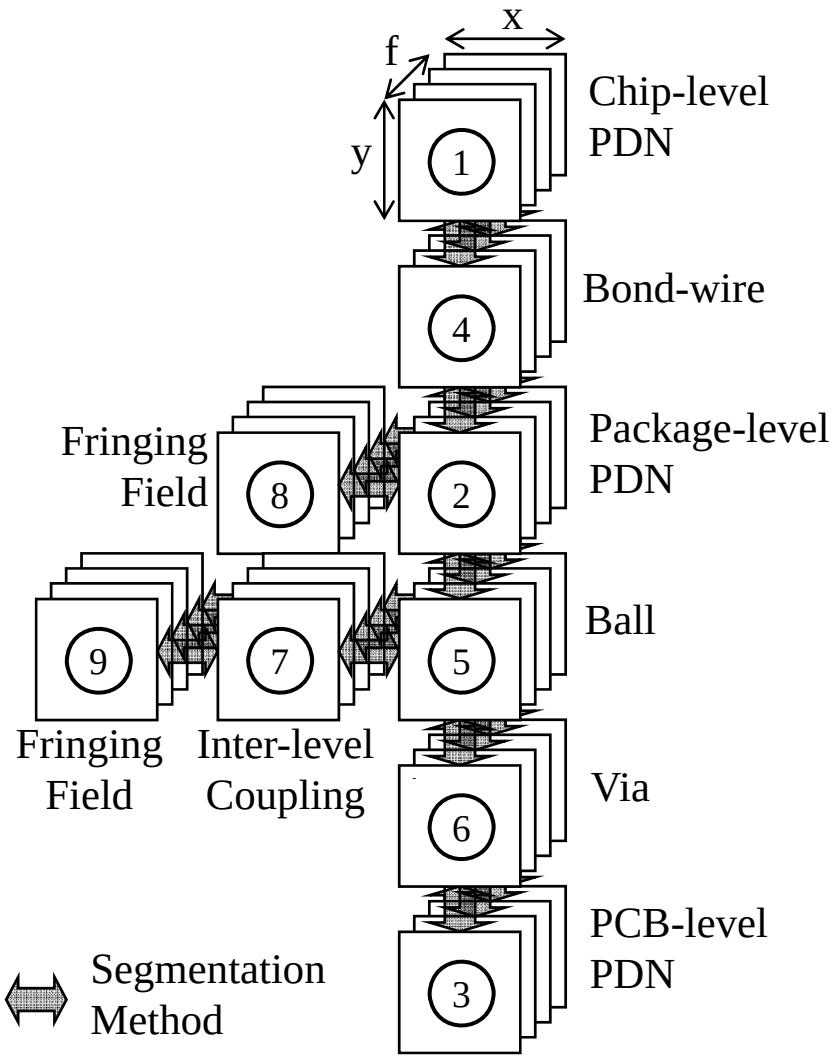
- **SSN was almost suppressed with High-DK thin film embedded capacitor**

PDN Design Methods

- Frequency dependent capacitance and inductance control
- Increase of decoupling Capacitance depending frequency range (on-chip, on-package, on-PCB, lumped, embedded)
- Decrease of Inductance (line, plane, via, wire, bonds, decoupling capacitors)
- Control resonances (lumped, planar cavity, on-chip, inter-level): avoid overlap with clock and harmonic frequencies
- Control ESR to reduce peak resonance impedance
- Evaluate dc ESR for dc voltage drop estimation

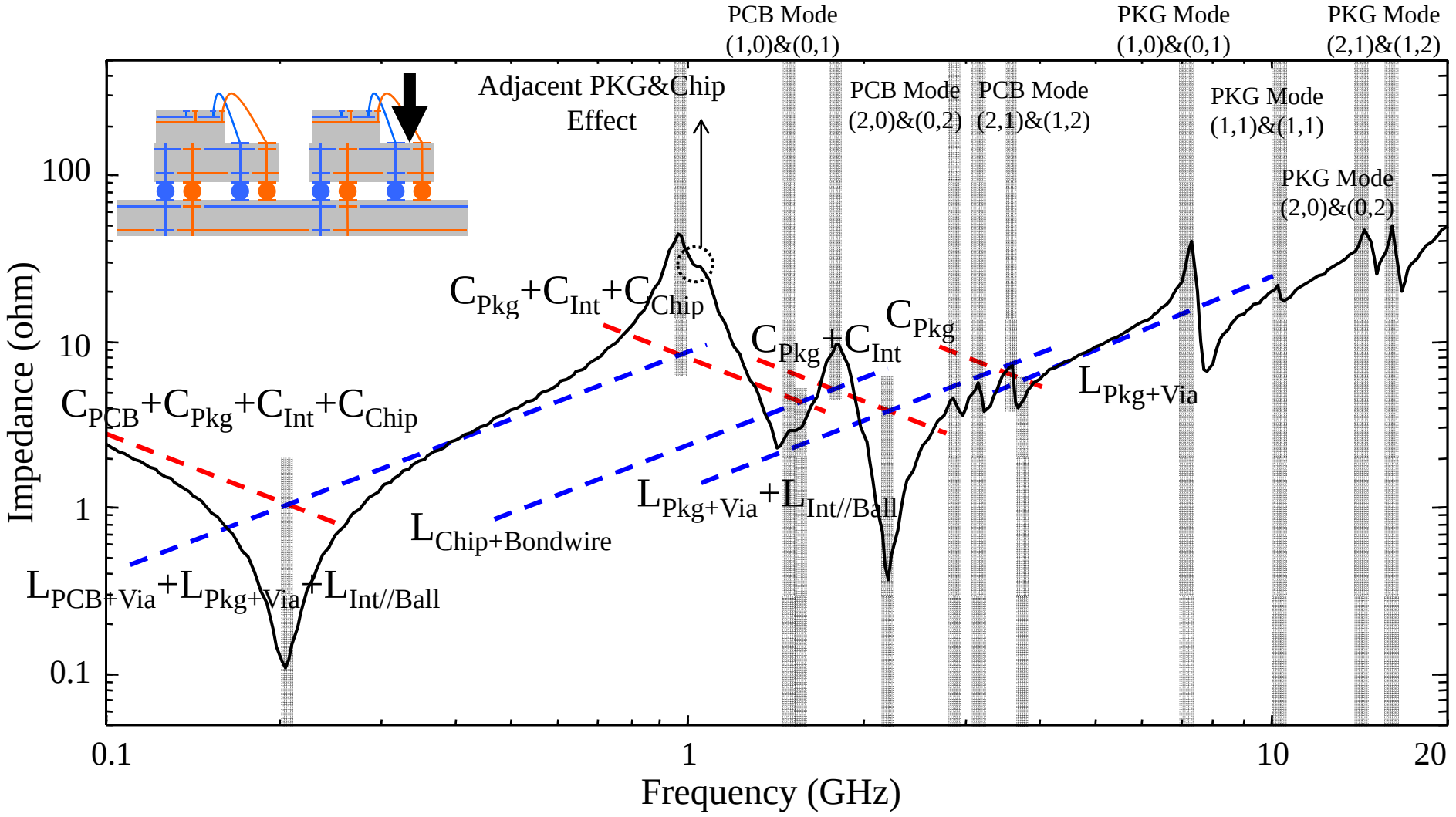
Proposed Modeling Method for Chip-Package-PCB Hierarchical PDN





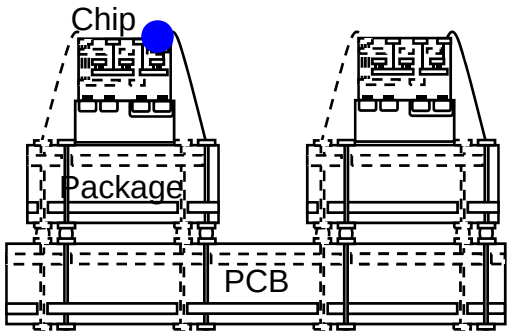
✓ Considering all parts in hierarchical PDN and merging them into one using segmentation method

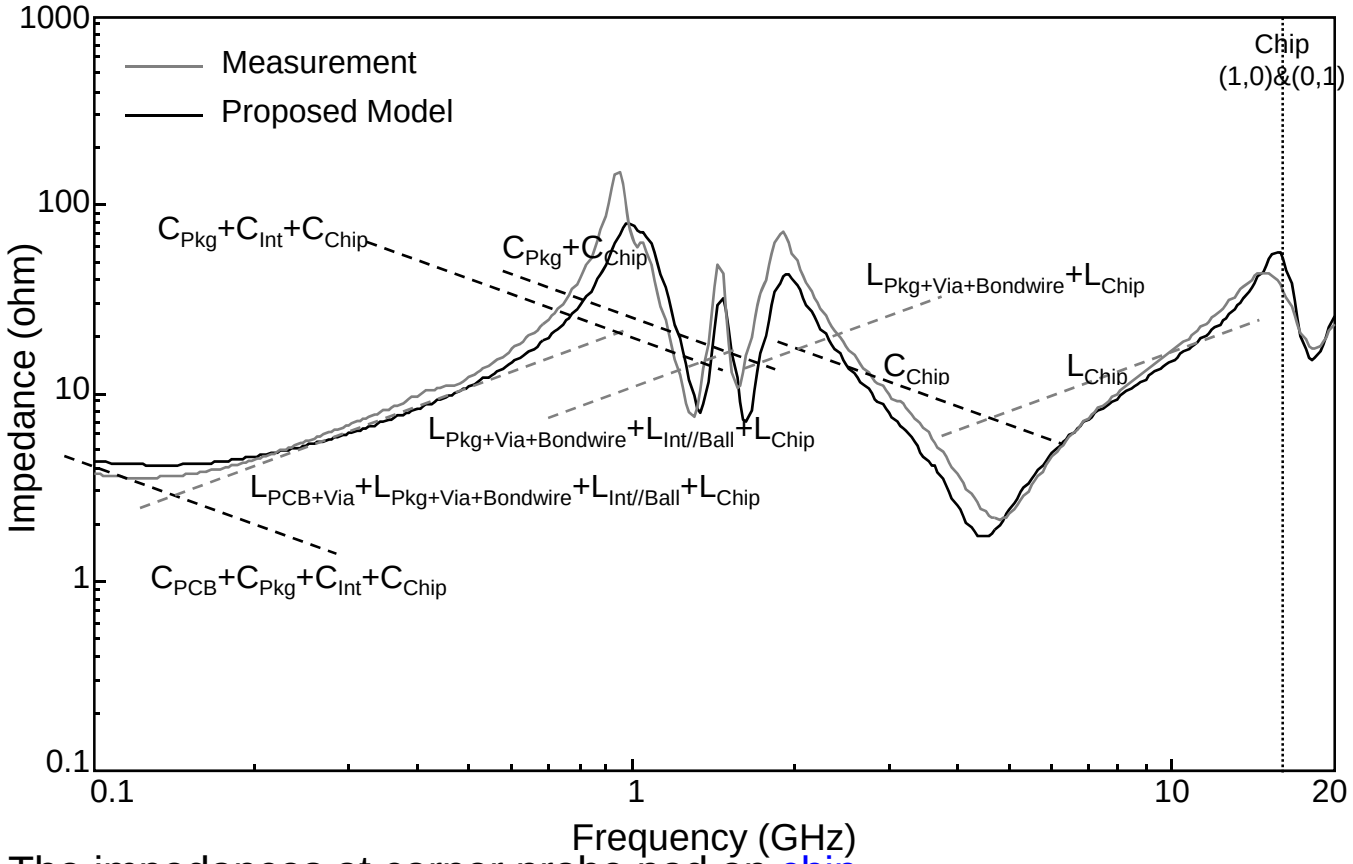
Analysis of Impedance of Test Vehicle at Package Side



✓ A quite complicated impedance characteristic composed of chip-package-PCB hierarchical PDN is fully analyzed.

Verification of Proposed Modeling Method (Corner on Chip)





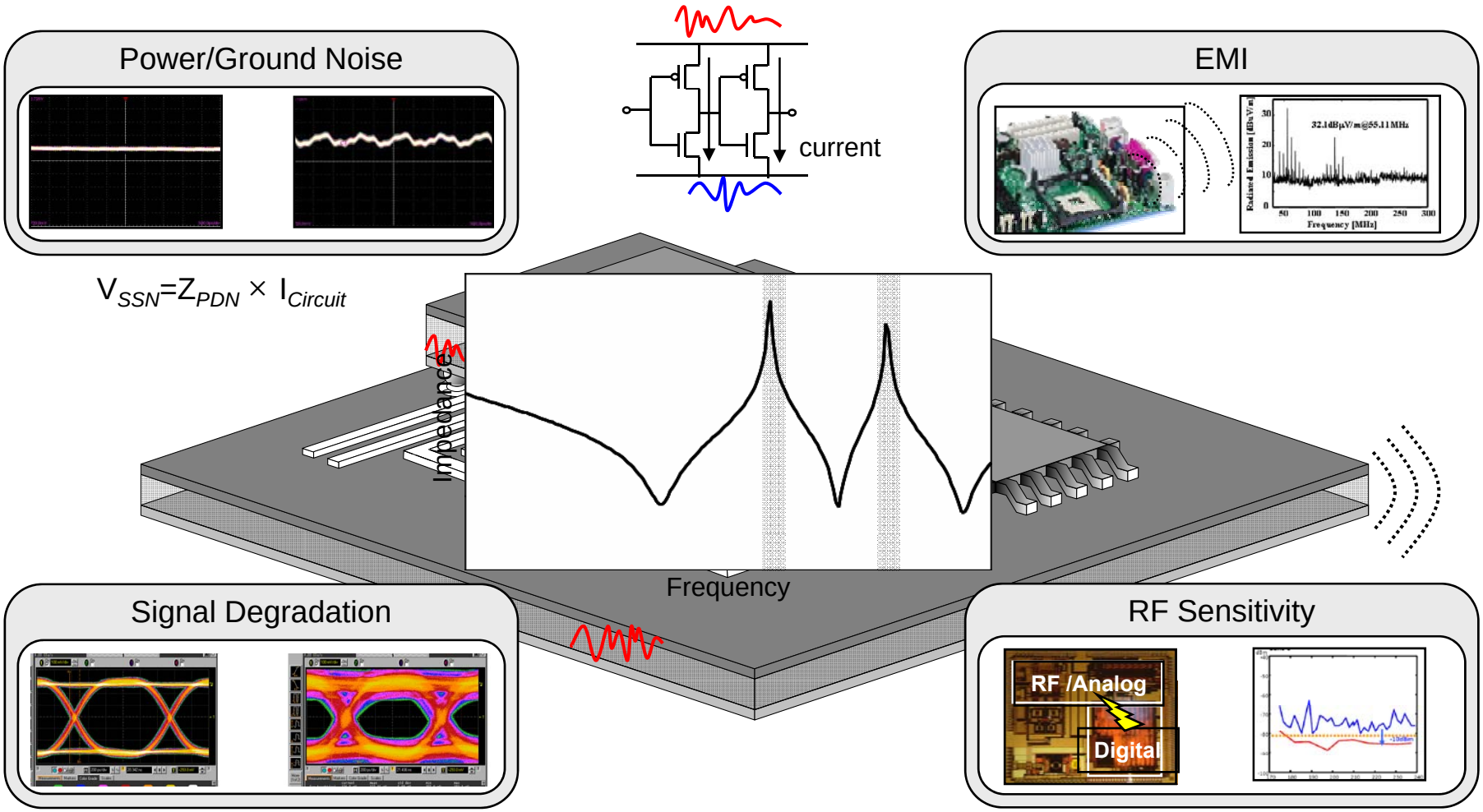
- The impedances at corner probe pad on chip
- Frequency : 100MHz to 20GHz
- 5 high impedance peaks

  4 peaks → interactions

  1 peak → mode resonance of chip

Need for Estimation of High Impedance Peak in Hierarchical PDN

- High impedances in hierarchical PDN from interactions generate problems of system performance degradation.

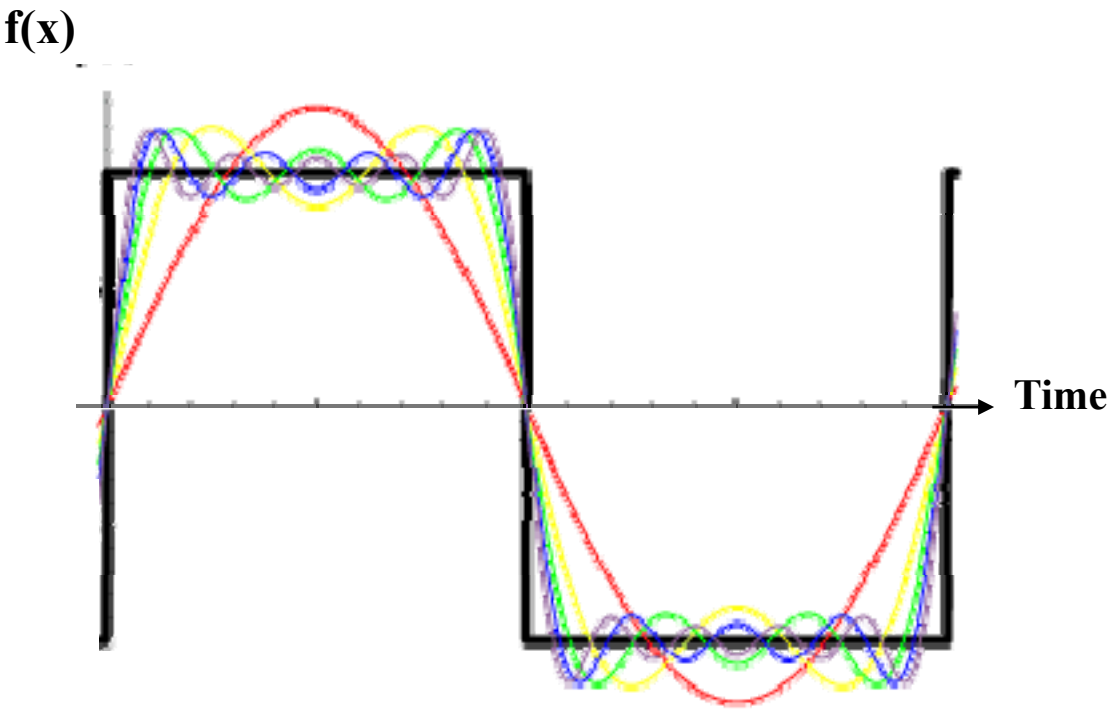


- A precise simulation and analysis of hierarchical PDN is needed.

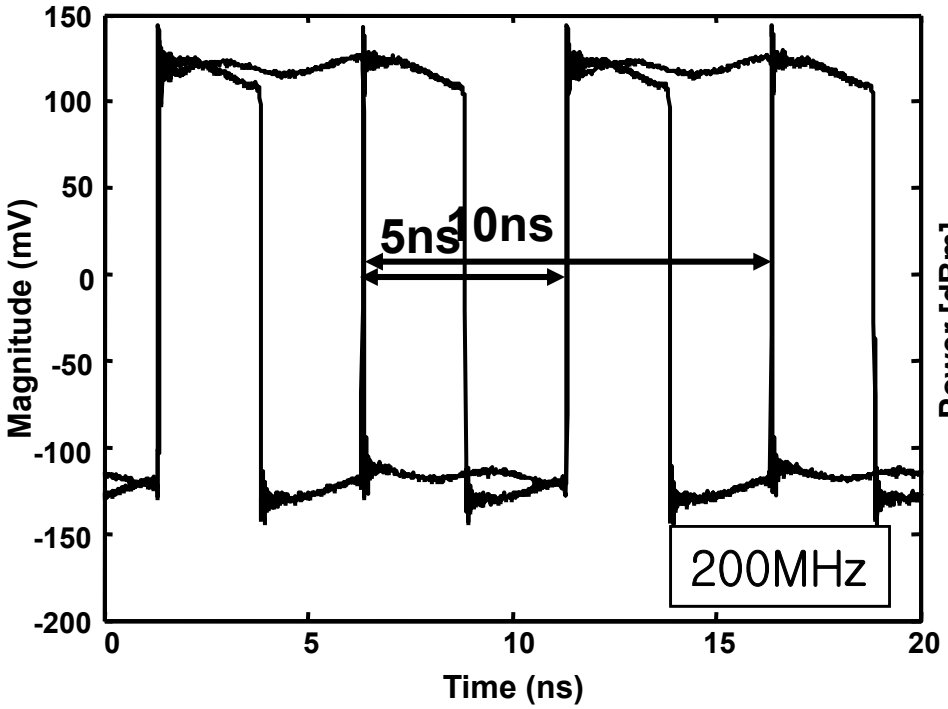
PDN Noise Coupling Paths in chip and package

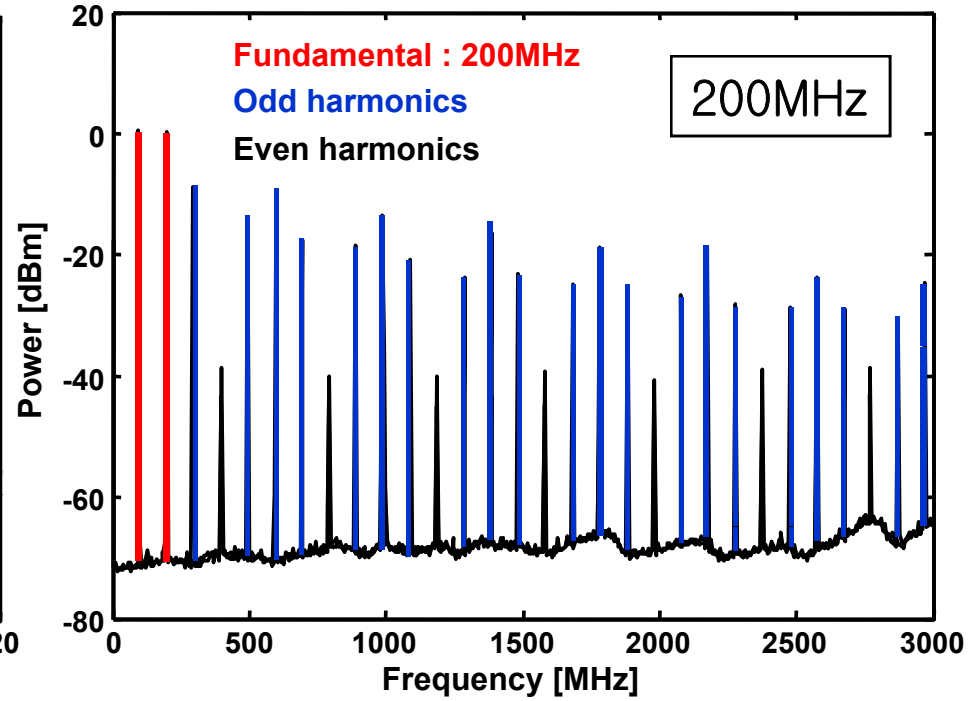
- Adjacent interconnections: line, pin, wire
- Via and planes
- Conductive substrates
- Common power line, plane
- Common decoupling capacitors
- Common return current paths
- Isolation techniques needed: Cost, size increase

Frequency Spectrum of Digital Clock Waveforms

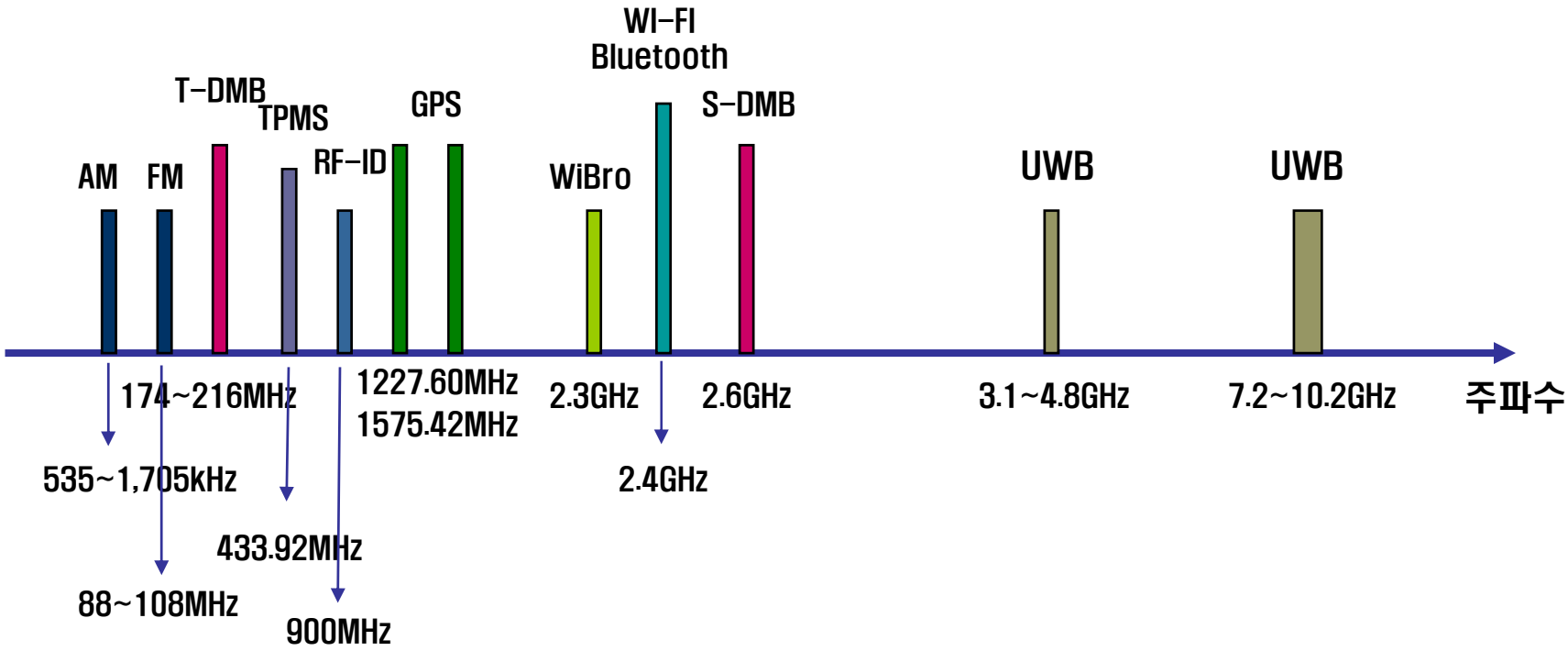


Waveform and Spectrum of Clock Signal

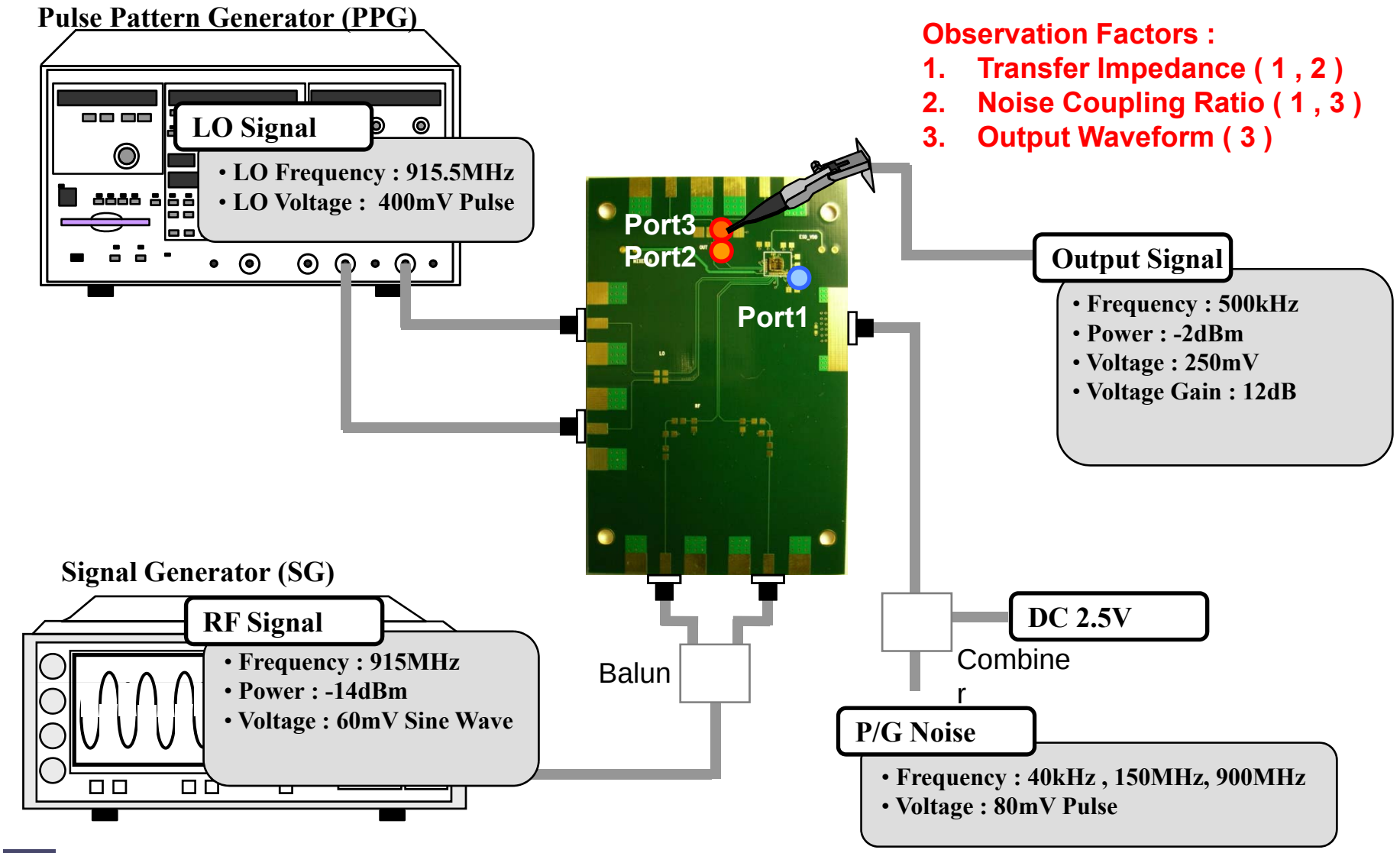




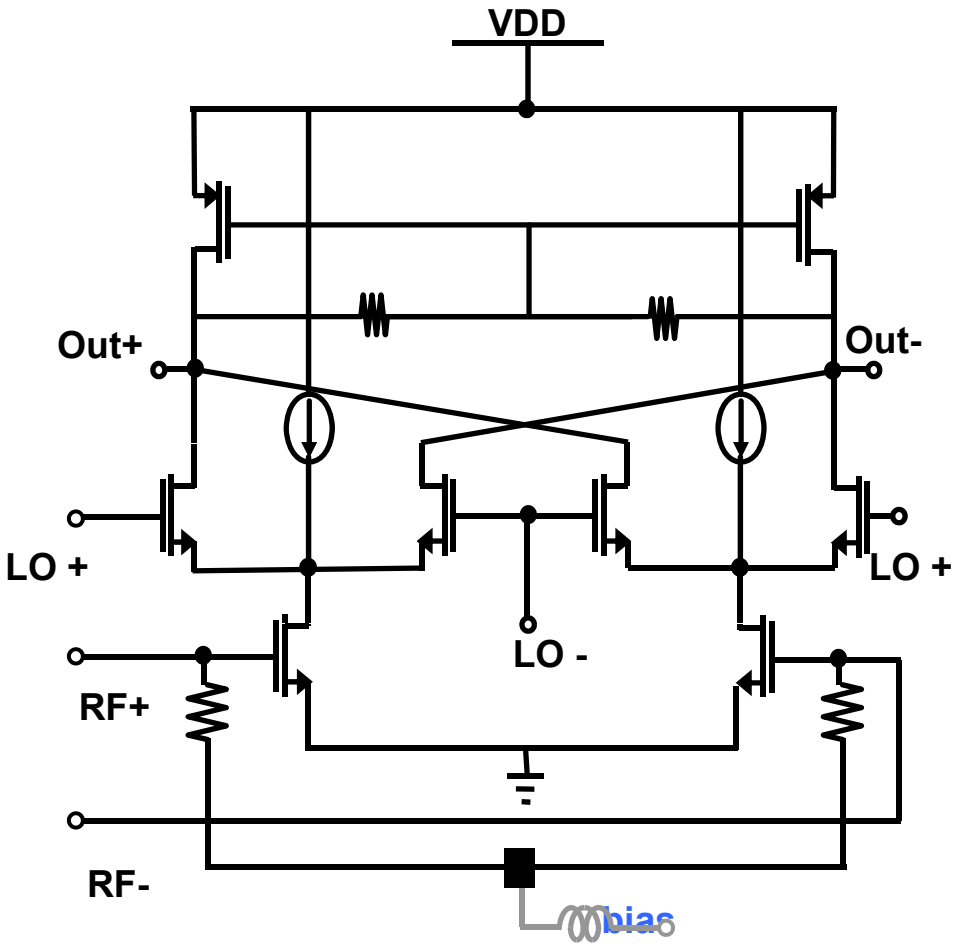
Spectrum of Wireless Mobile Communication Systems



Setup for Analysis

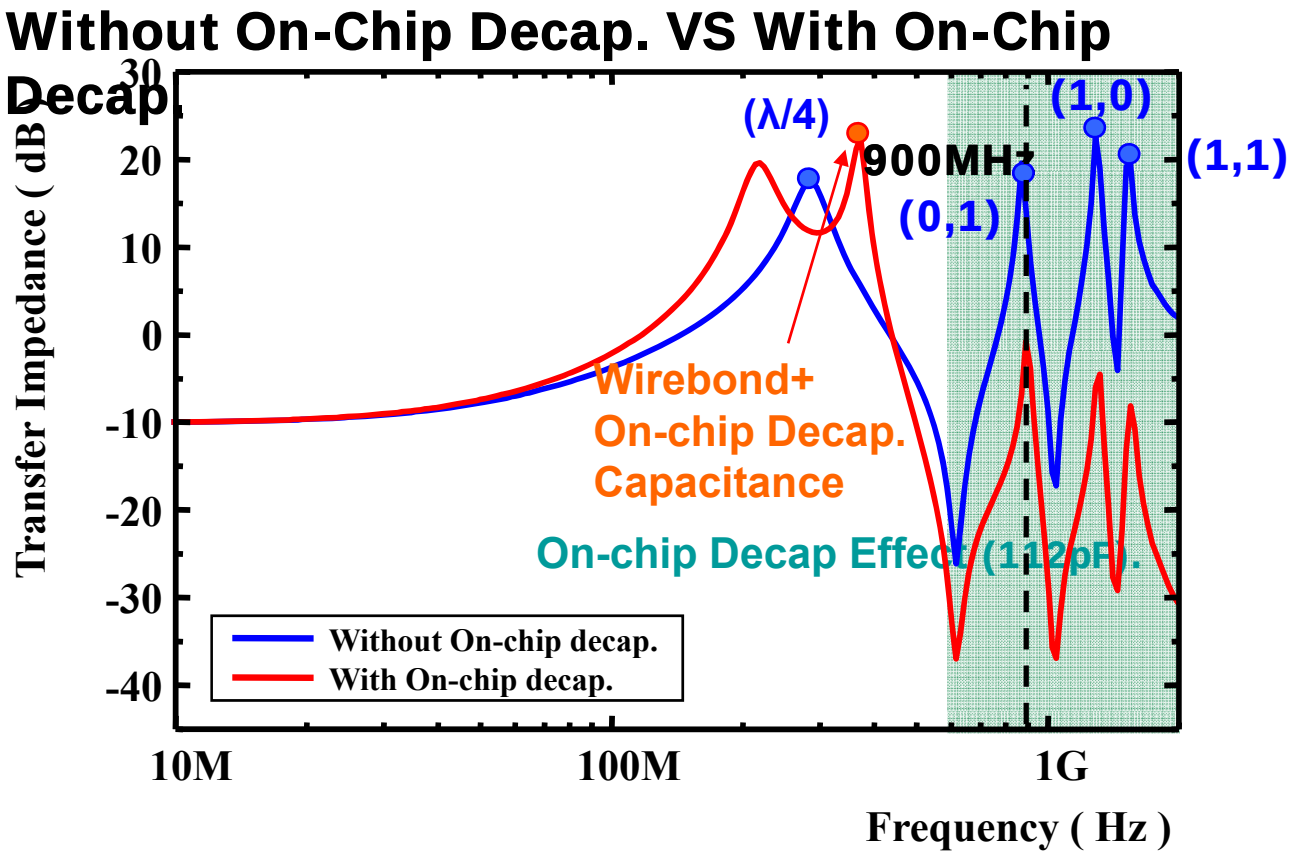


Basic Performance of Designed Mixer



- Double Balanced Mixer
- TSMC 0.25um Process
- Target Frequency : 860 ~ 960 MHz
- Gain : 10 ~ 12 dB
- P1dB : - 5dBm
- RF Isolation : -30dB
- LO Isolation : -25dB
- Direct Conversion Frequency : 500kHz

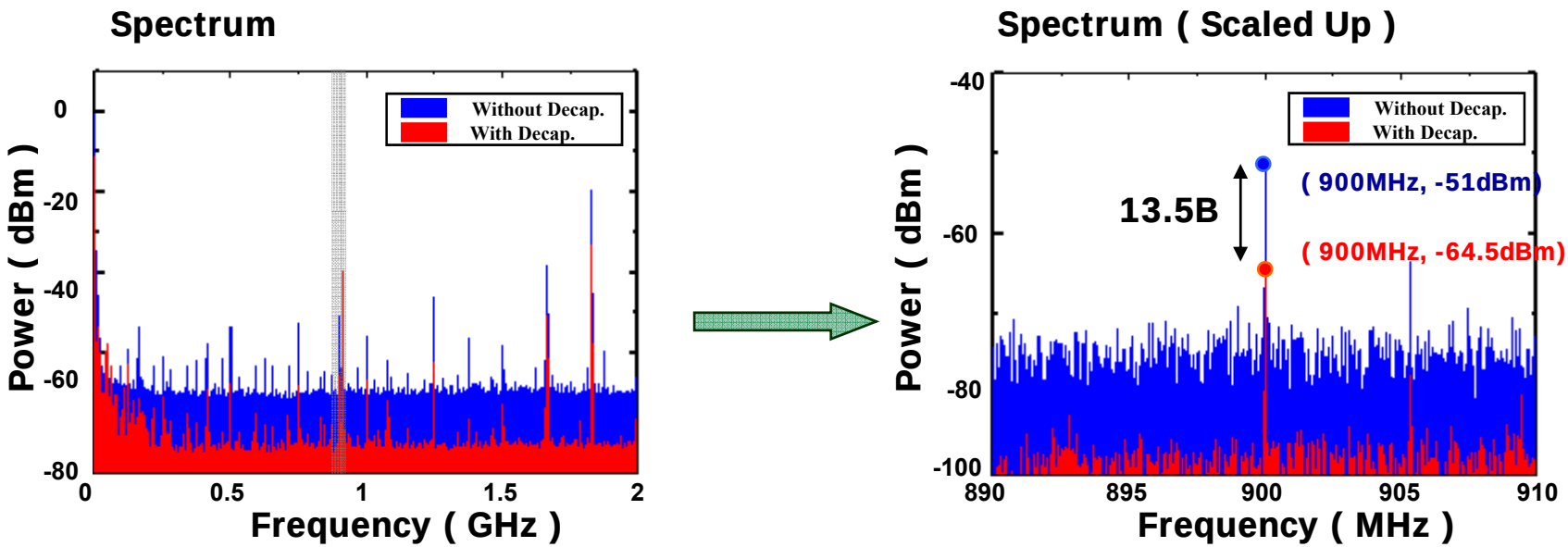
On-chip Decap. Effect : Transfer Impedance (Simulation)



- When on-chip decoupling capacitor is designed , transfer impedance decreases more than the case without on-chip decoupling capacitor over 600MHz

- > Transfer impedance decreases when design on-chip decoupling capacitor in 900MHz.

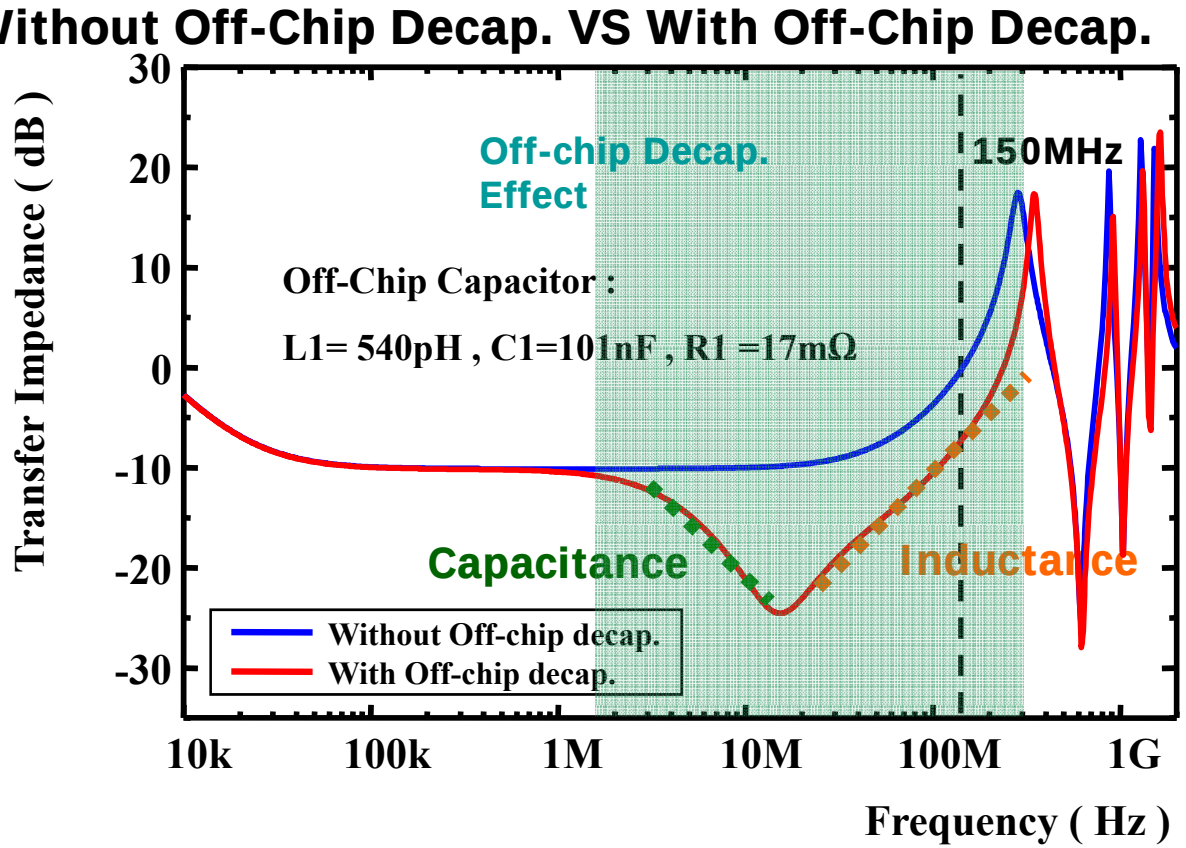
On-chip Decap. Effect : Output Spectrum (Measurement)



- Switching noise of output waveform with on-chip decoupling capacitor decreases in 13.5dB a frequency of 900MHz compared to the case without on-chip decoupling capacitor .

  -> Verified effect of design on-chip decoupling capacitor in RF or LO frequency band.

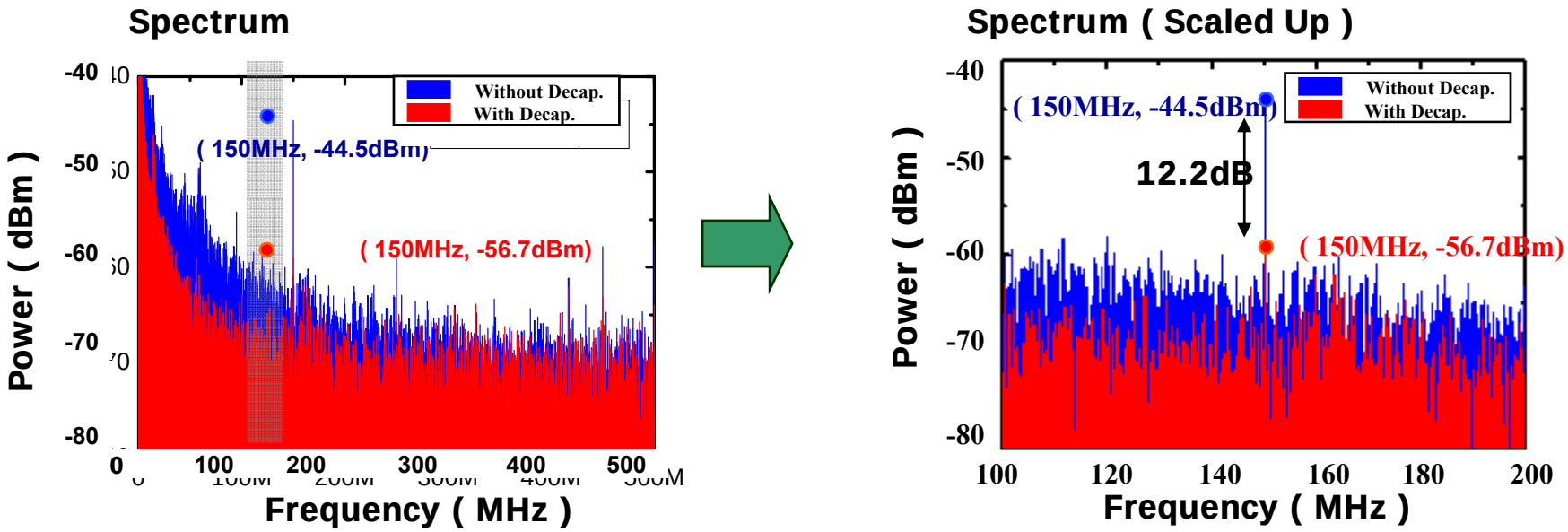
Off-chip Decap. Effect : Transfer Impedance (Simulation)



- When additional off-chip decoupling capacitor is designed , transfer impedance decreases more than the case without additional off-chip decoupling capacitor from 2MHz to 200MHz

- > Transfer impedance decreases when design on-chip decoupling capacitor in 150MHz.

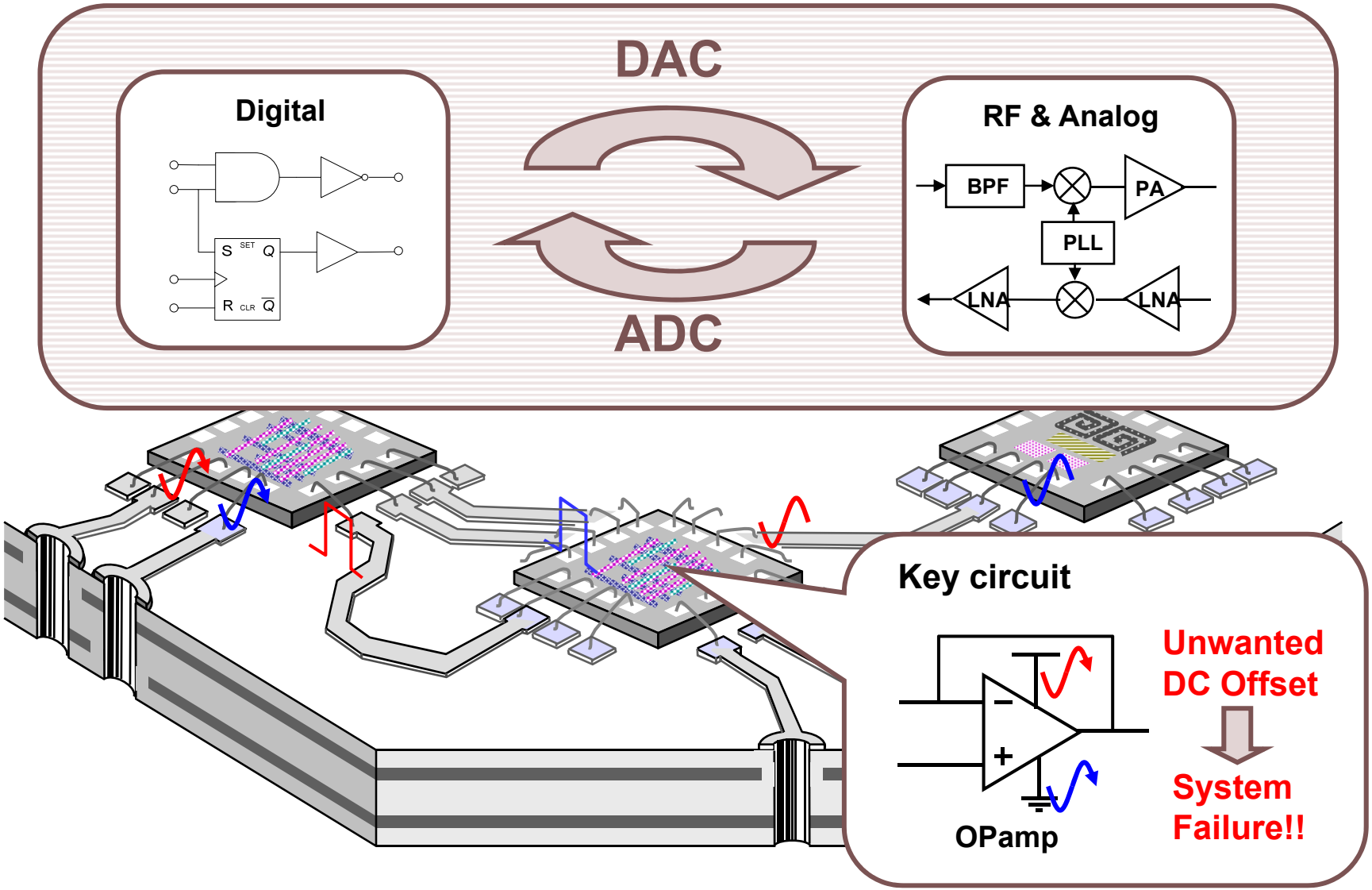
Off-chip Decap. Effect : Output Spectrum (Measurement)



- Switching noise of output waveform with off-chip decoupling capacitor decreases in 12.2dB a frequency of 150MHz compared to the case without off-chip decoupling capacitor .

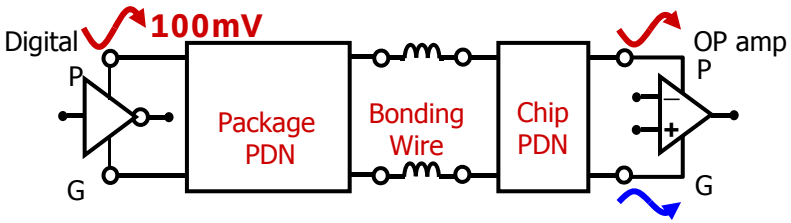
  -> Verified effect of design off-chip decoupling capacitor in IF frequency band.

Problem by Power and Ground Noise

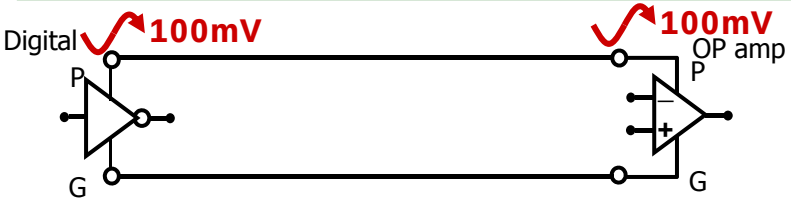


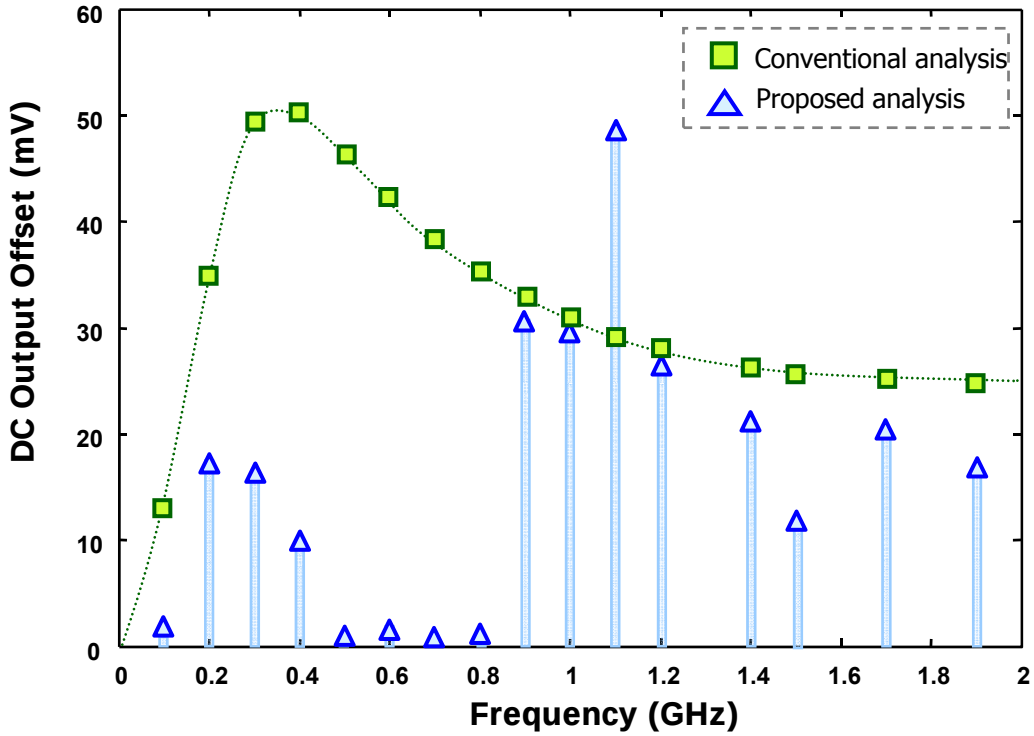
DC Output Offset with Proposed and Conventional Analysis

DC Output Offset with Proposed Analysis



DC Output Offset with Conventional Analysis





Considerable Distinction between DC Output Offset with and without Consideration of PDN

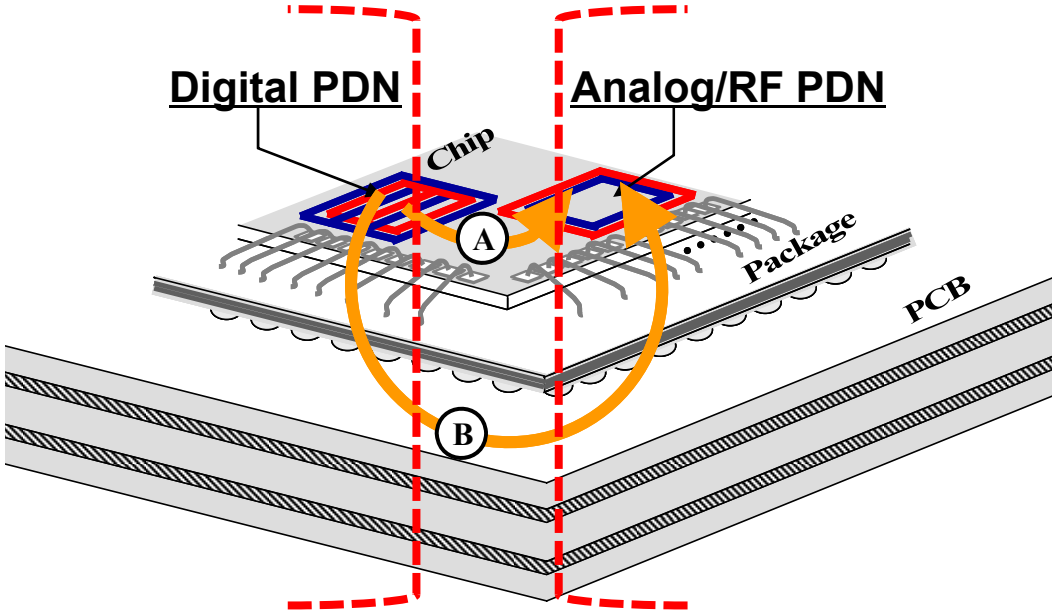
SSN Sensitive Circuits in IC

- VCO: Voltage Controlled Oscillator
- LNA: Low Noise Amplifier
- PLL: Phase Locked Loop
- ADC: Analog to Digital Converter
- DAC: Digital to Analog Converter

SSN Isolation Methods

- Decoupling
- Filtering
- Slot
- Split
- Shielding
- EBG strictures
- Separated power supply/decoupling/return current path
- Separated interconnections: lines, pins, pads, vias
- Separated planes, layers
- Increased separation distance

PDN Noise Isolation Methods



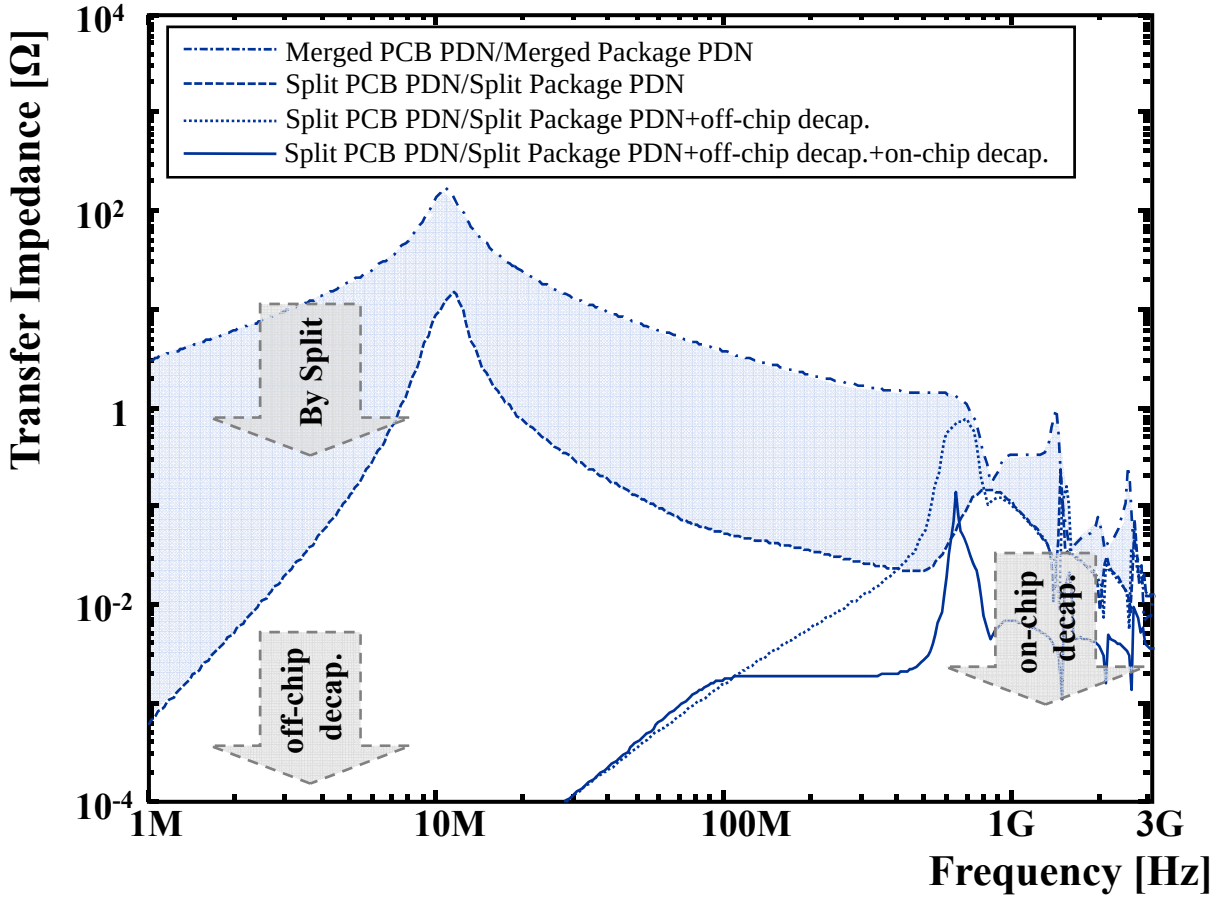
Ⓐ Chip Level
- Split On-chip Metal PDN Bus
- Guard Ring (P+/ N+/ Deep-Nwell type)
- On-chip Decoupling Capacitor
- Internal Voltage Regulator

Ⓑ Package/PCB Level
- Split Power/Ground Planes
- On-Package/PCB Decoupling Capacitor (Discrete type, Embedded type)
- Electromagnetic Band Gap (EBG)

→ **Frequency dependency of noise isolation**

→ **Z21 analysis in the frequency domain**

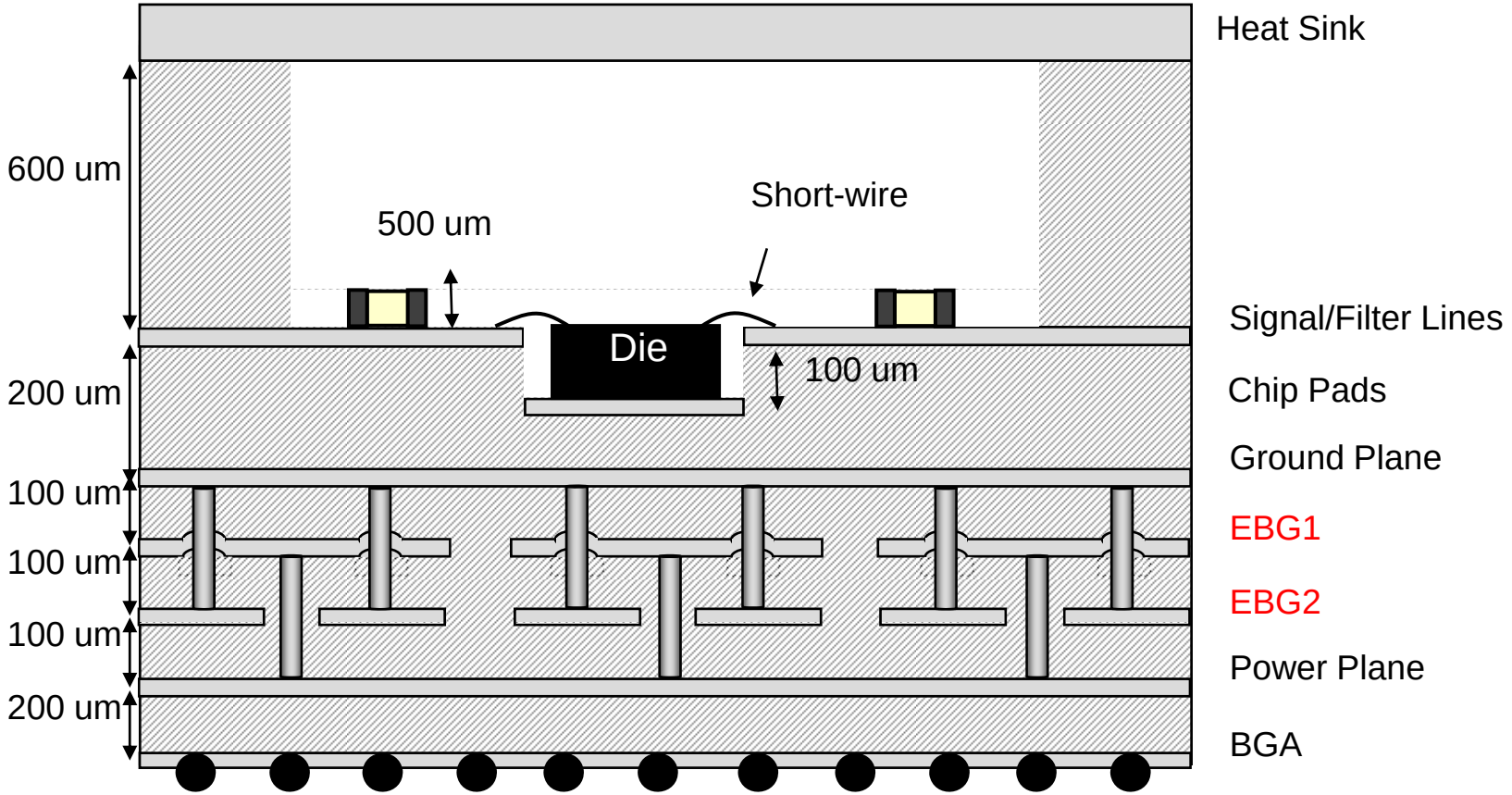
The isolation methods of each hierarchical PDN



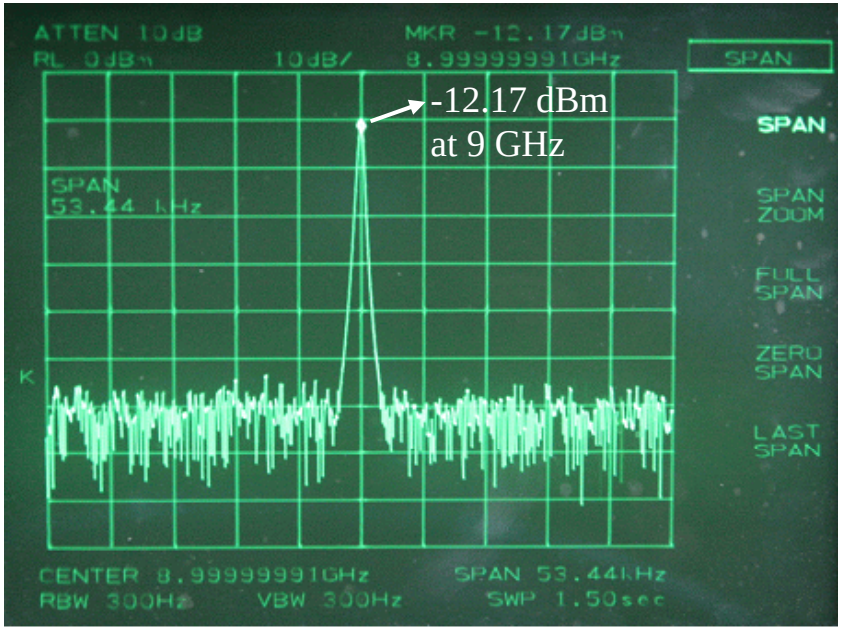
• By split of PCB and package level PDN,
the PDN transfer impedance can be suppressed except around 10MHz.
• By adding on-/off-chip decoupling capacitor,
the PDN transfer impedance can be suppressed in both low and high frequency region.

Stack-up for Transceiver SiP [7 layer]

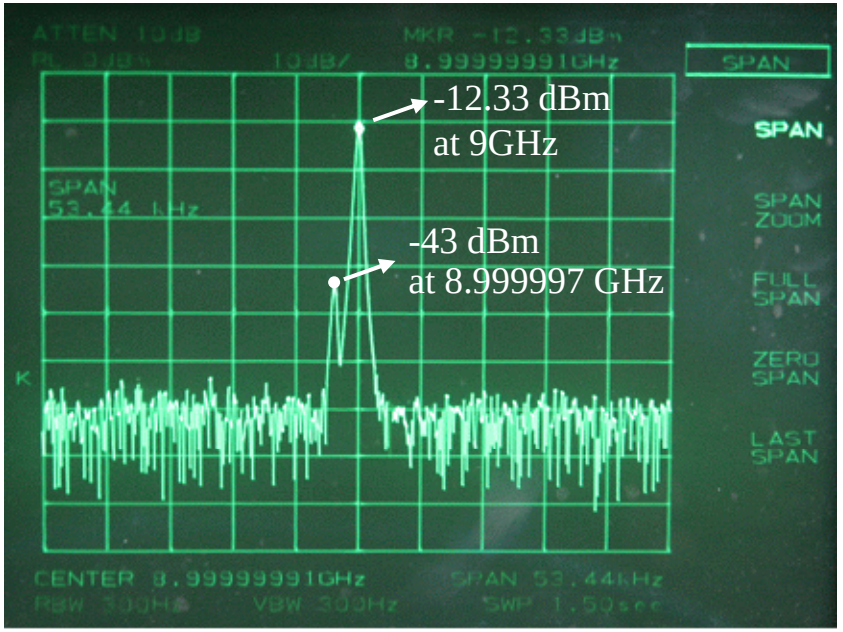
- Thickness = 1.3 mm, Size: 20mmx20mm,
- Ceramic: Dupont (Dielectric Constant = 7.4, Loss Tangent = 0.001)
- Die: 7, Decap: 5 개, Ball: 287, Wire-bonding: 53 개
- 7 Layers



Transceiver without DS-EBG



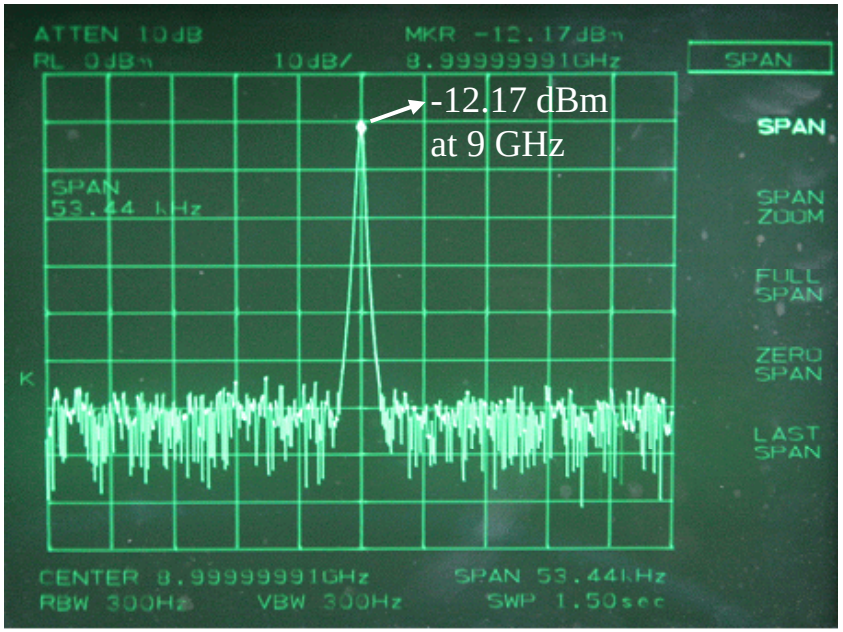
< Without Power/Ground Noise >



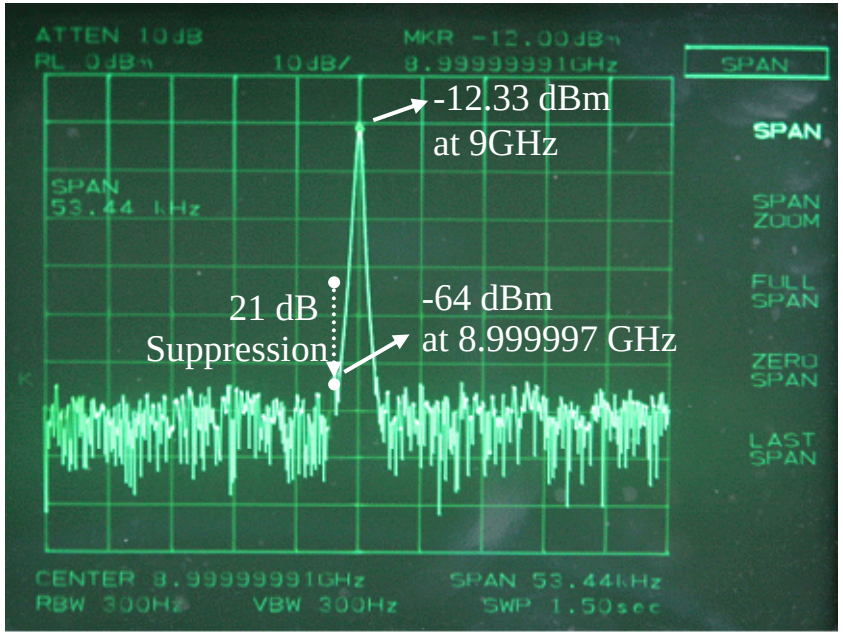
< With Power/Ground Noise >

- Power/Ground noise generates a -43 dBm of unwanted signal near the output signal.

Transceiver with DS-EBG



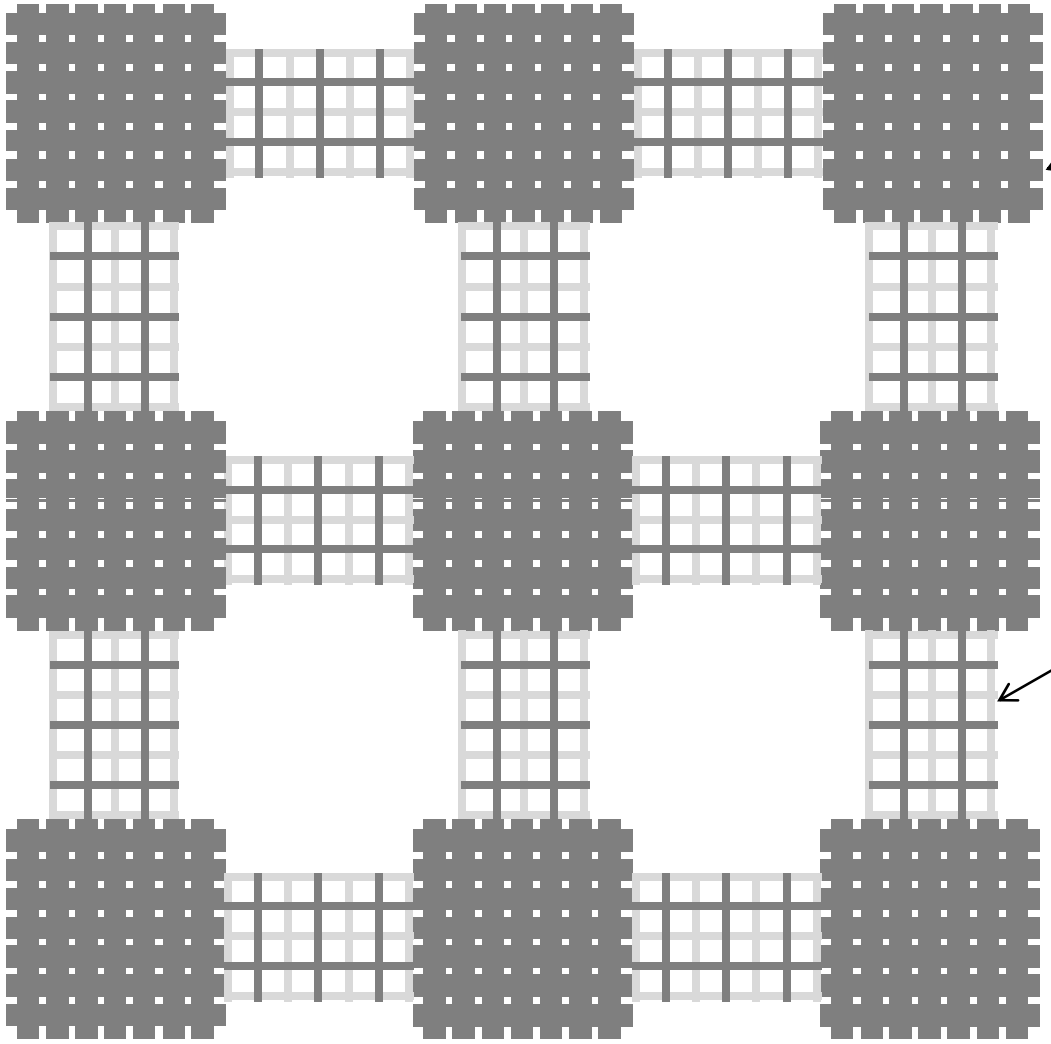
< Without Power/Ground Noise >



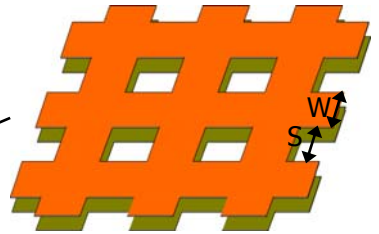
< With Power/Ground Noise >

- DS-EBG successfully suppresses the unwanted signal by 21 dB.

Proposed On-Interposer EBG Structure



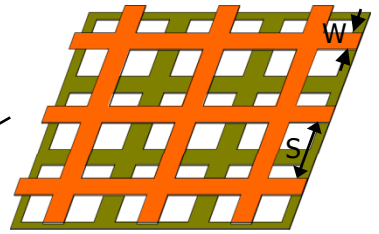
Capacitive P/G mesh



Width: 80um

Space: 120um

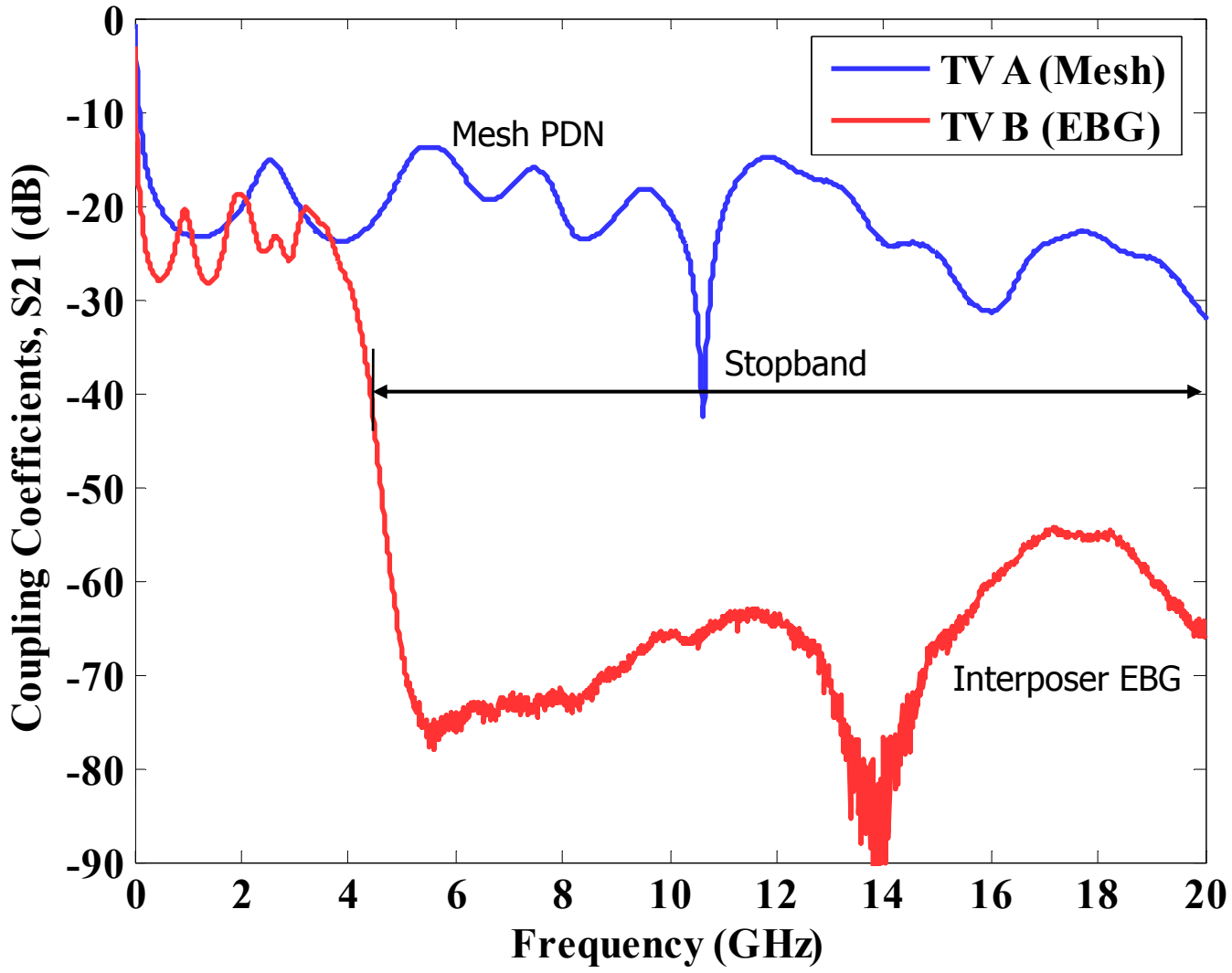
Inductive P/G mesh



Width: 40um

Space: 360um

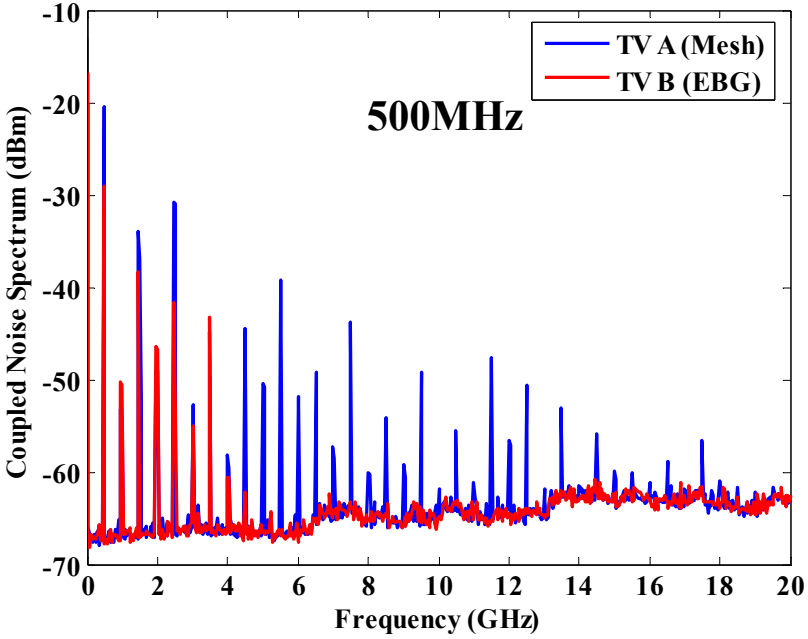
Measurement Results (1/2)

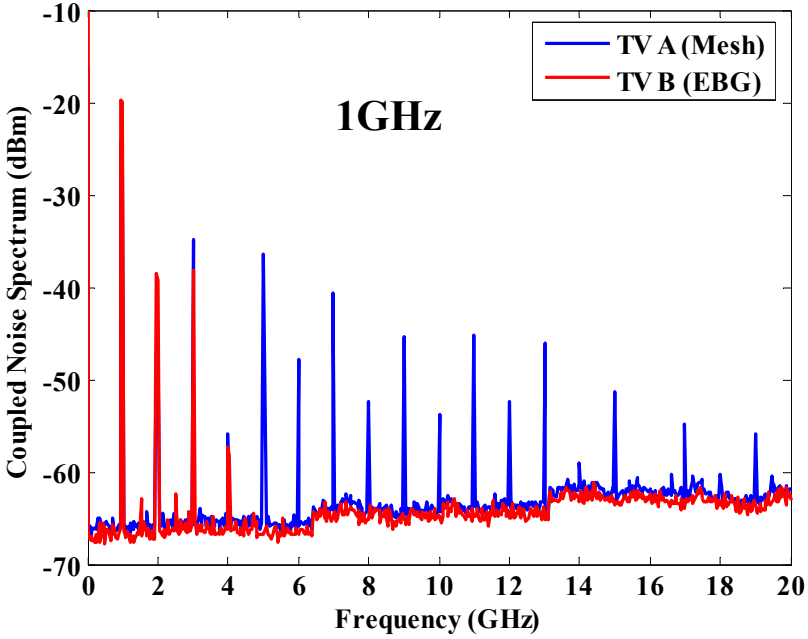


Measurement Results (2/2)

- Switching noise input at port 1 using 500mVpp clock signal

- Coupled noise spectrum probed at port 2

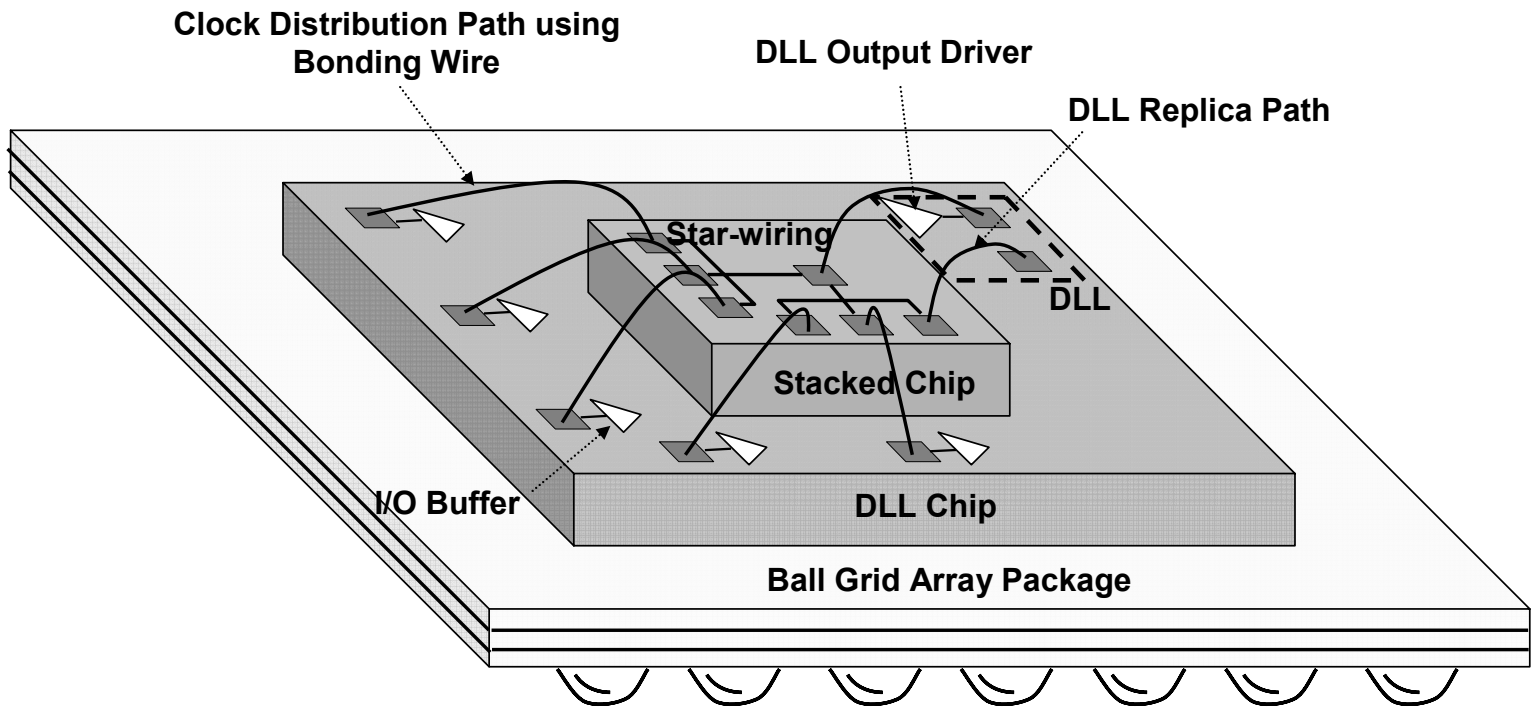




Proposed 3D Clock Distribution Scheme

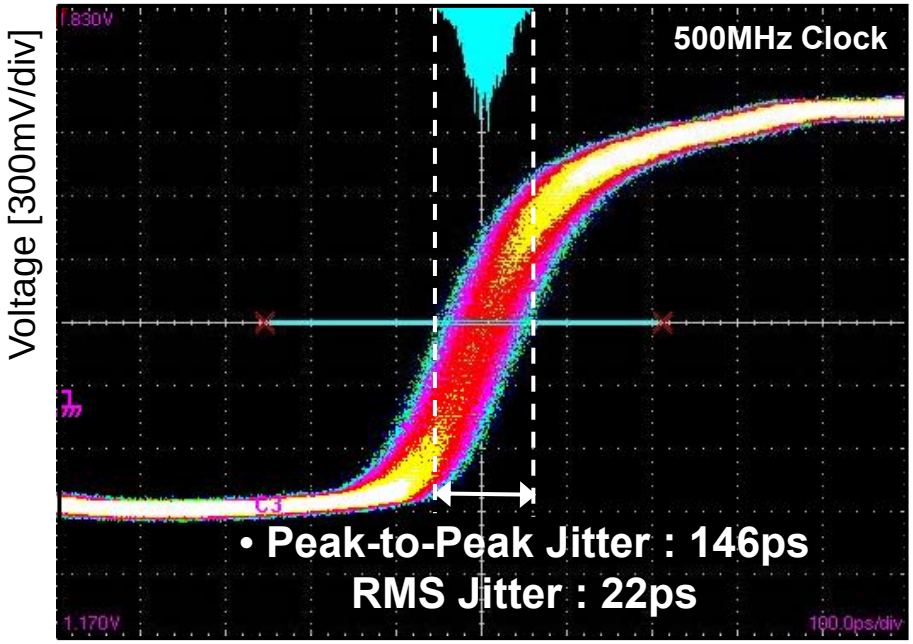
3-D Stacked Chip Star-wiring I/O Clock Distribution for Low Jitter, Skew, and Delay

➔ lossless of bonding-wire & pad
➔ free from on both on chip and package power supply noise

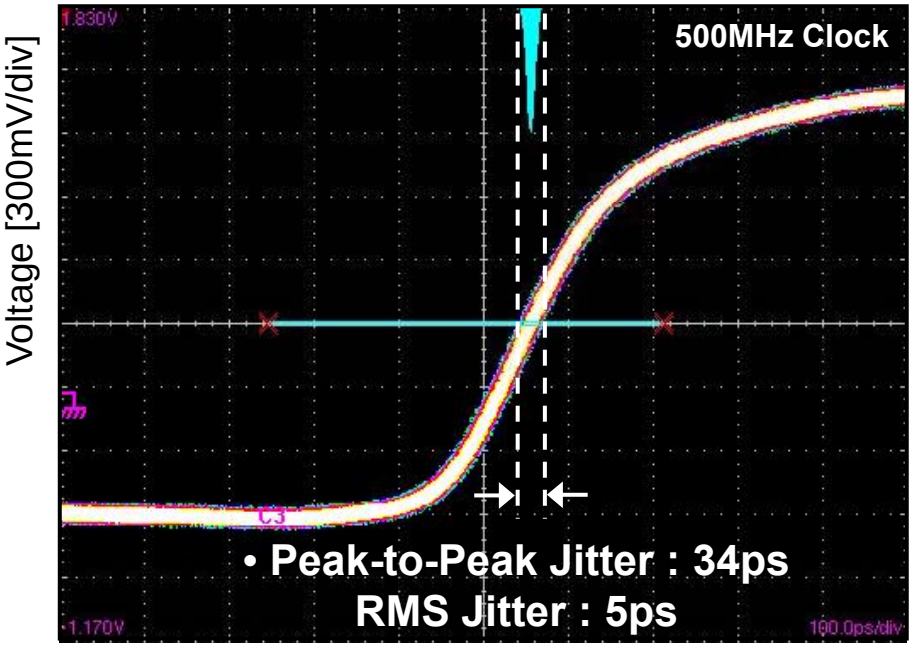


Enhanced Clock Jitter Performance of the Proposed Scheme

Conventional On-chip I/O Clock Distribution Scheme



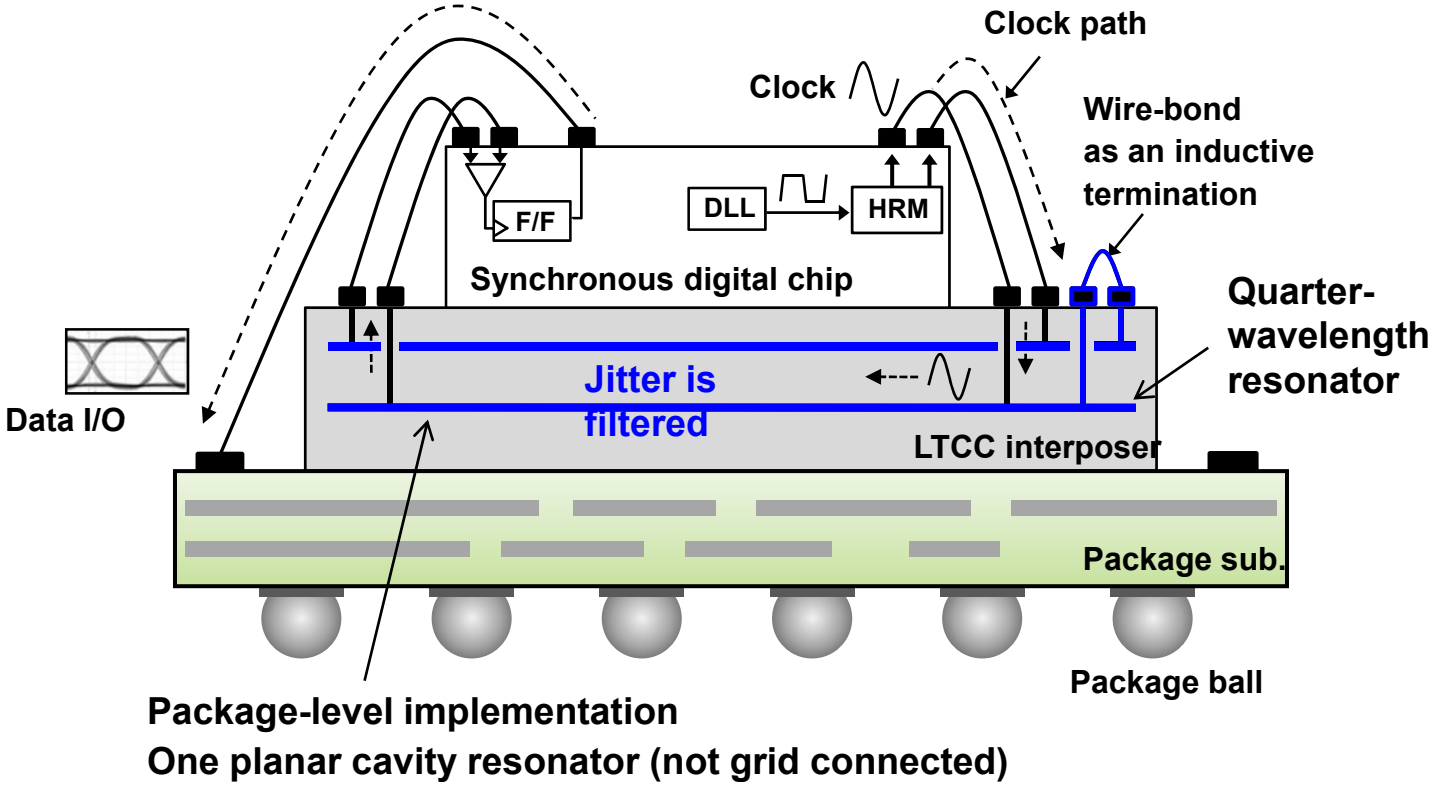
3D Stacked Chip Star-wiring I/O Clock Distribution Scheme



✓ **3D-stacked chip star-wiring clock scheme provides low clock jitter compared with on-chip clock scheme (77% jitter reduction)**

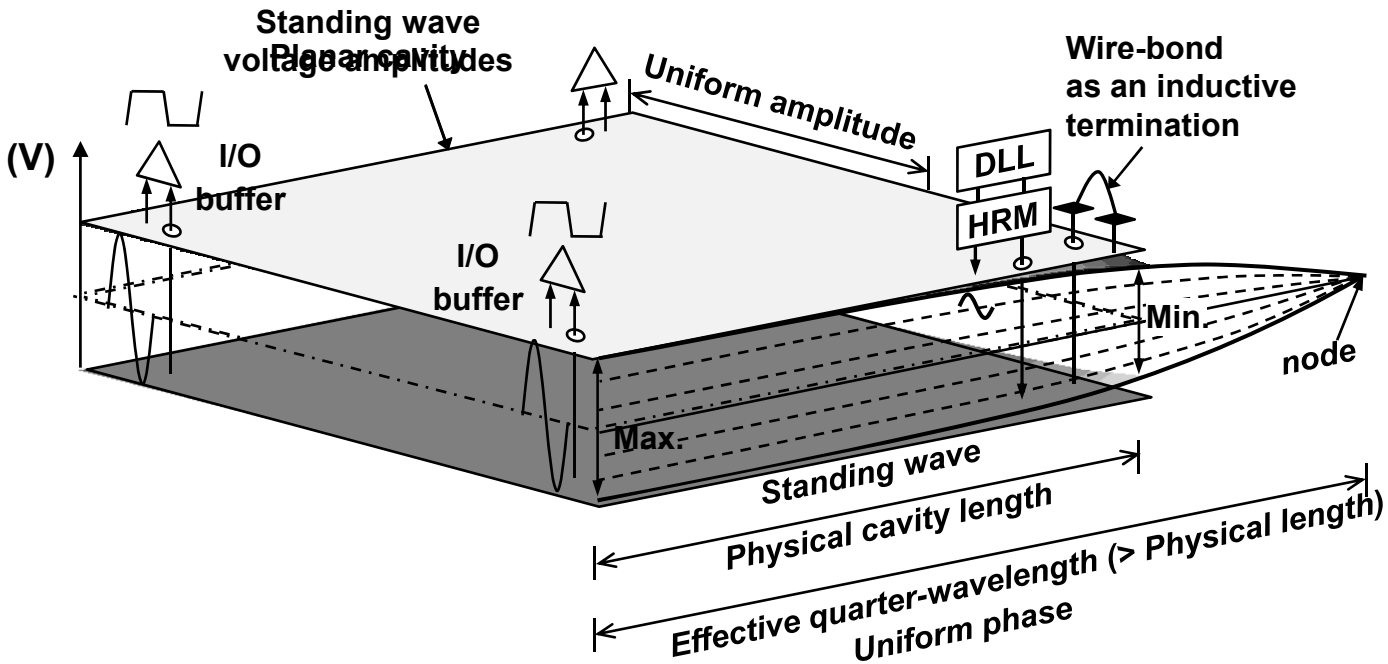
✓ **It is devised to enable the clock signal delivery to be free from on-chip digital switching noise and package power/ground cavity noise coupling.**

Advantages of Proposed PCR CDN for 3D Stacked Chip Package



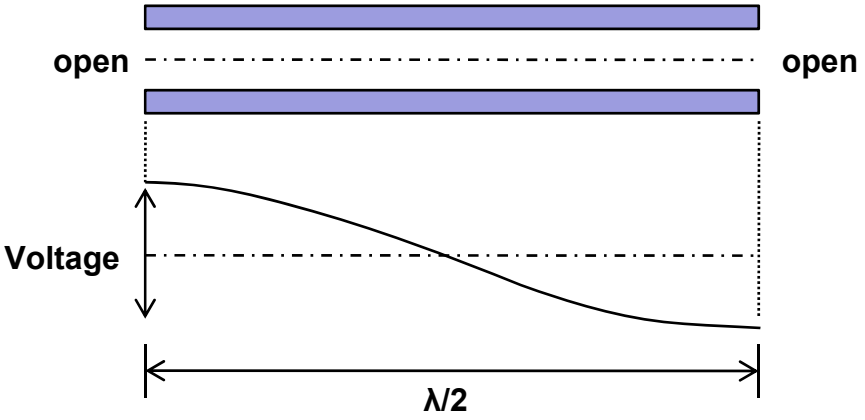
- Jitter is filtered by high-Q bandpass filter utilizing a package level quarter-wavelength planar cavity resonator
- Reduction of the number of cascaded repeaters

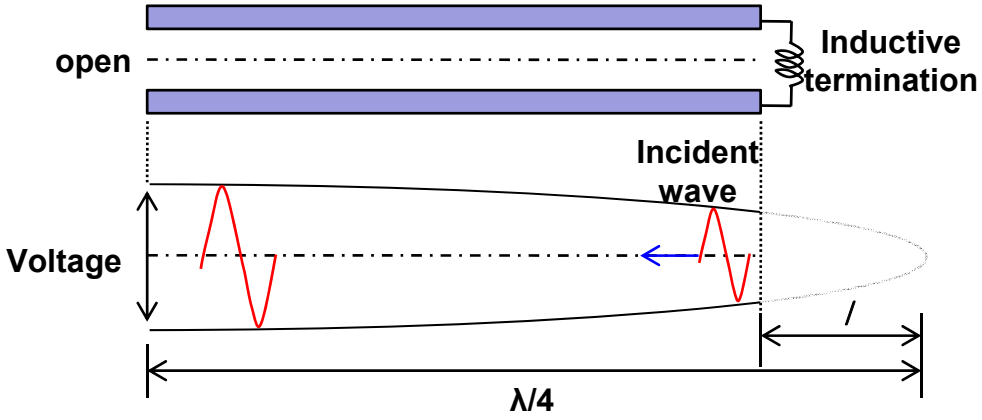
Originalities of Proposed PCR CDN for 3D Stacked Chip Package

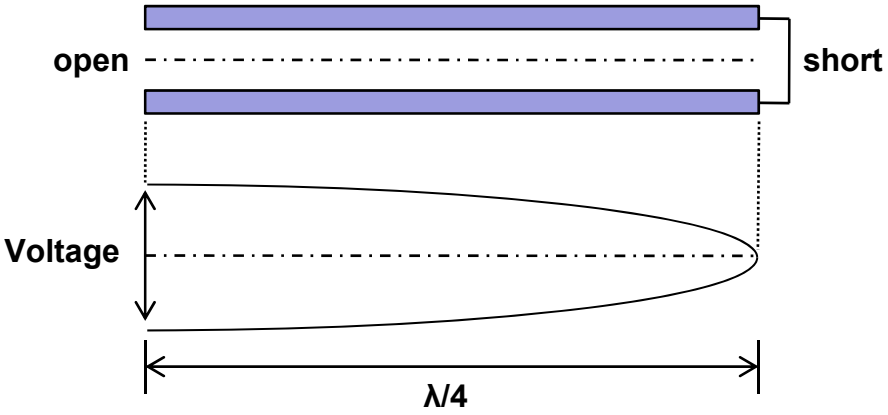


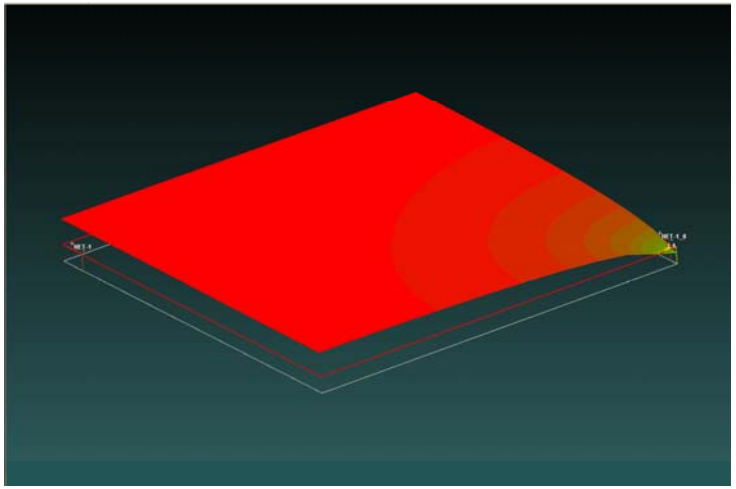
- **Uniform phase and uniform amplitude standing wave is used for clock distribution**

Quarter-wavelength Resonator with Inductive Termination



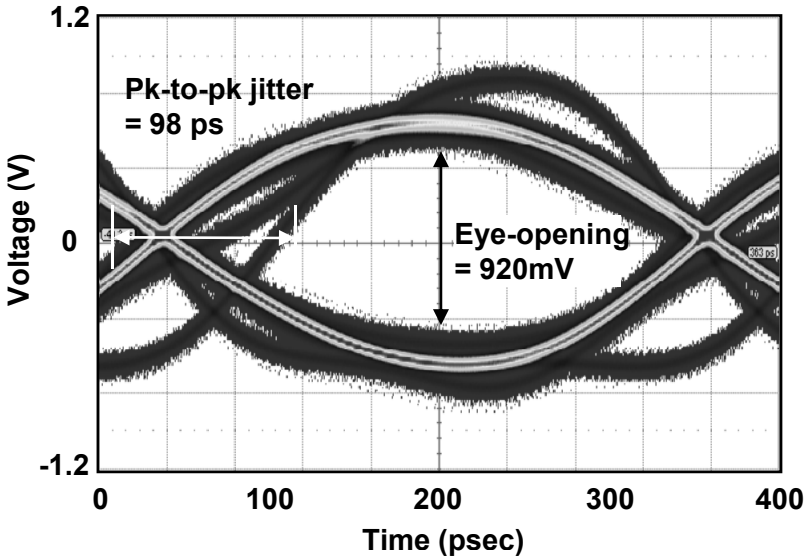




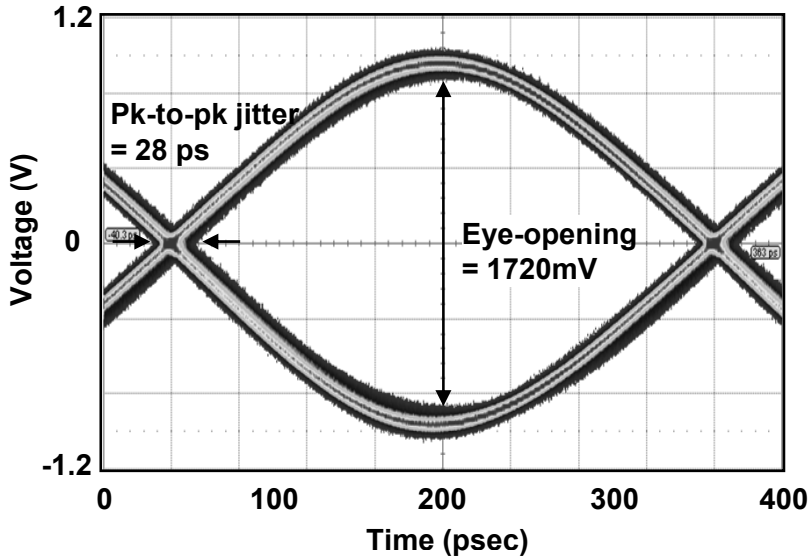


Measure Eyd-diagram of PCR CDN with Noise

Clock source before distribution



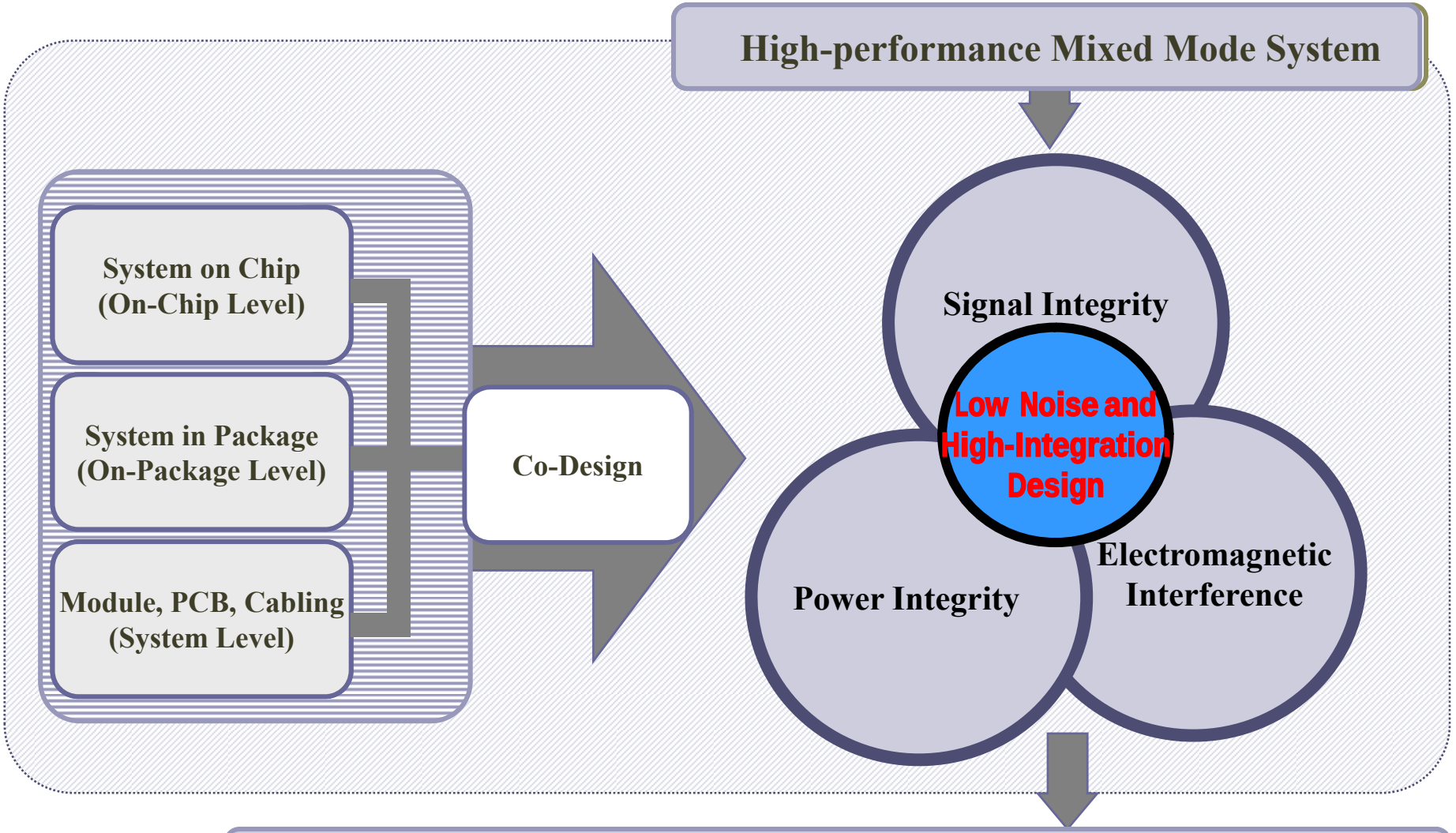
Distrbuted clock
at planar cavity resonator output



	Source clock	Distrbuted clock
Pk-to-pk jitter	98 ps	28 ps
Eye-opening	920 mV	1720 mV

- **Clock frequnecy : 1.55 GHz**
- **Clock magnitude : 1 Vp-p**
- **Switching noise : 300 mV**

Unique Research Focus



Conclusion

- Significant noise coupling occurs from digital PDN to noise sensitive RF and analog circuits on a same SiP.
- The clock frequencies and harmonic frequencies should be placed away from the RF carrier frequencies.
- Low PDN impedance should be maintained.
- PDN resonance frequencies should be placed away not only from the clock frequencies, and their harmonic frequencies, but also from RF carrier frequencies.
- Via and wire are a major noise coupling path from digital PDN to noise sensitive circuits.
- Noise coupling reduction methods including using PDN design, frequency control, filtering, separation/isolation, decoupling, shielding, and grounding techniques.
- Case studies: LNA, Clock distribution network
- Chip-package co-design can provide optimal and cost-effective solutions.