IEEE EMC Society Distinguished Lecturer Seminar: Signal Integrity of TSV-Based 3D IC

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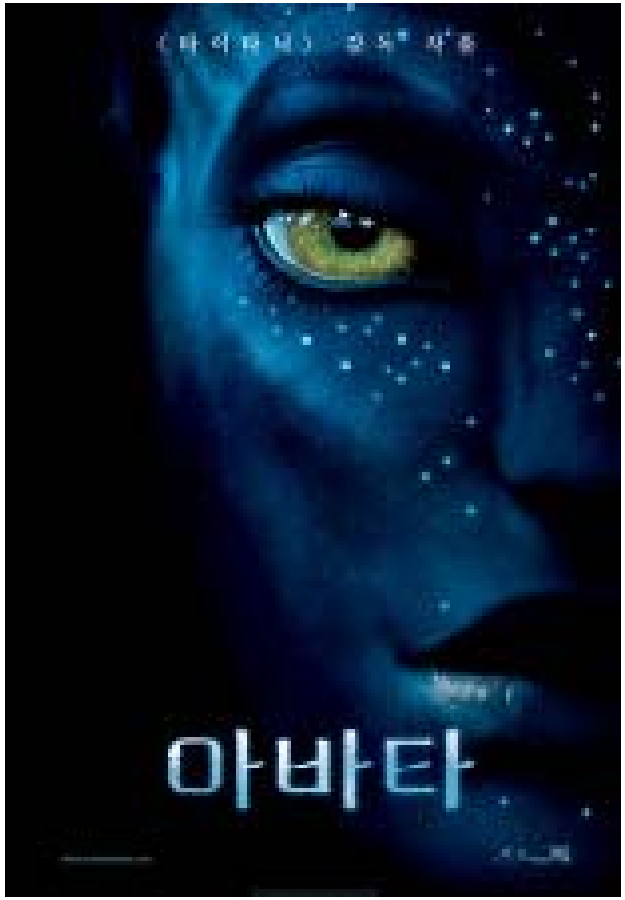
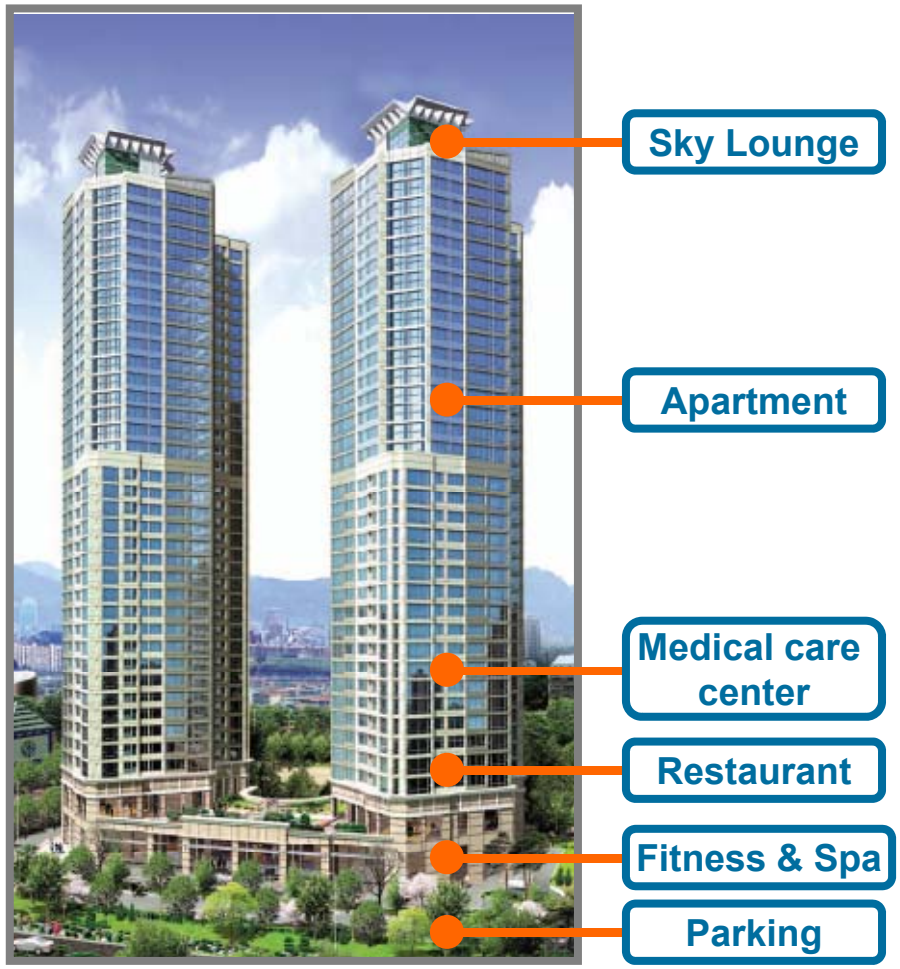
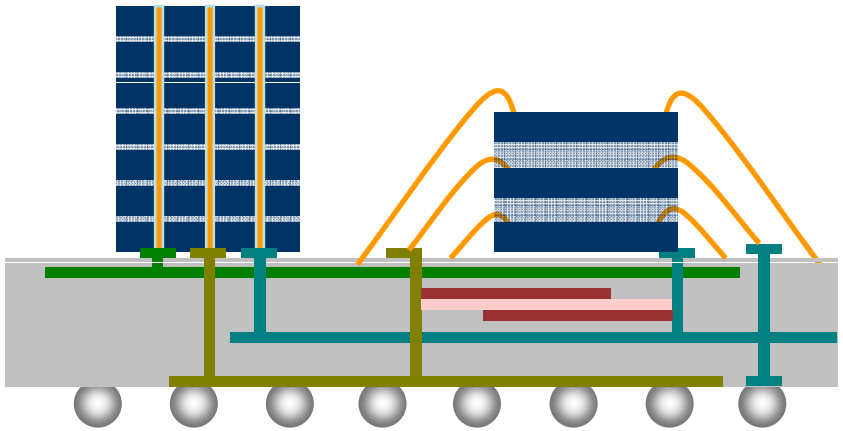
3D Movie

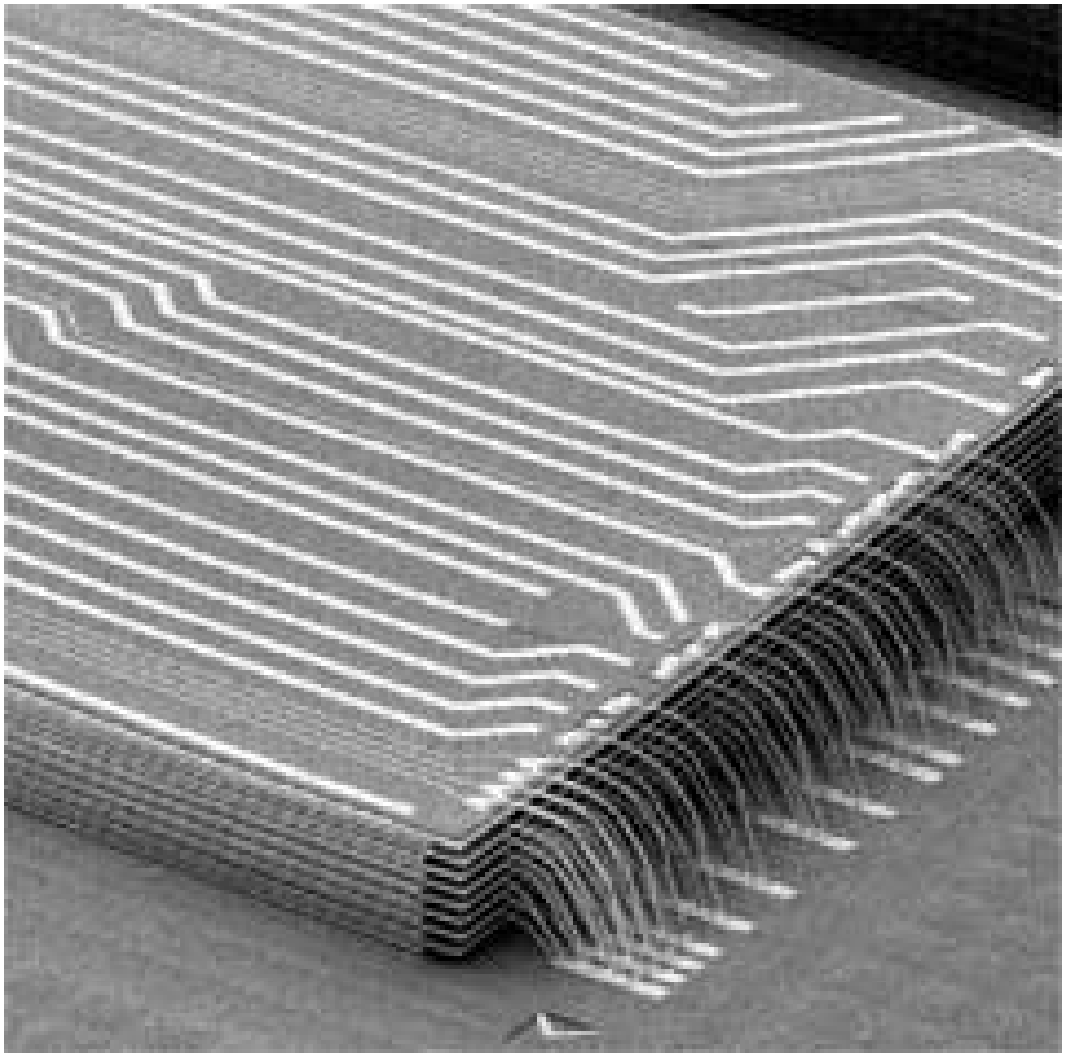


3D Housings

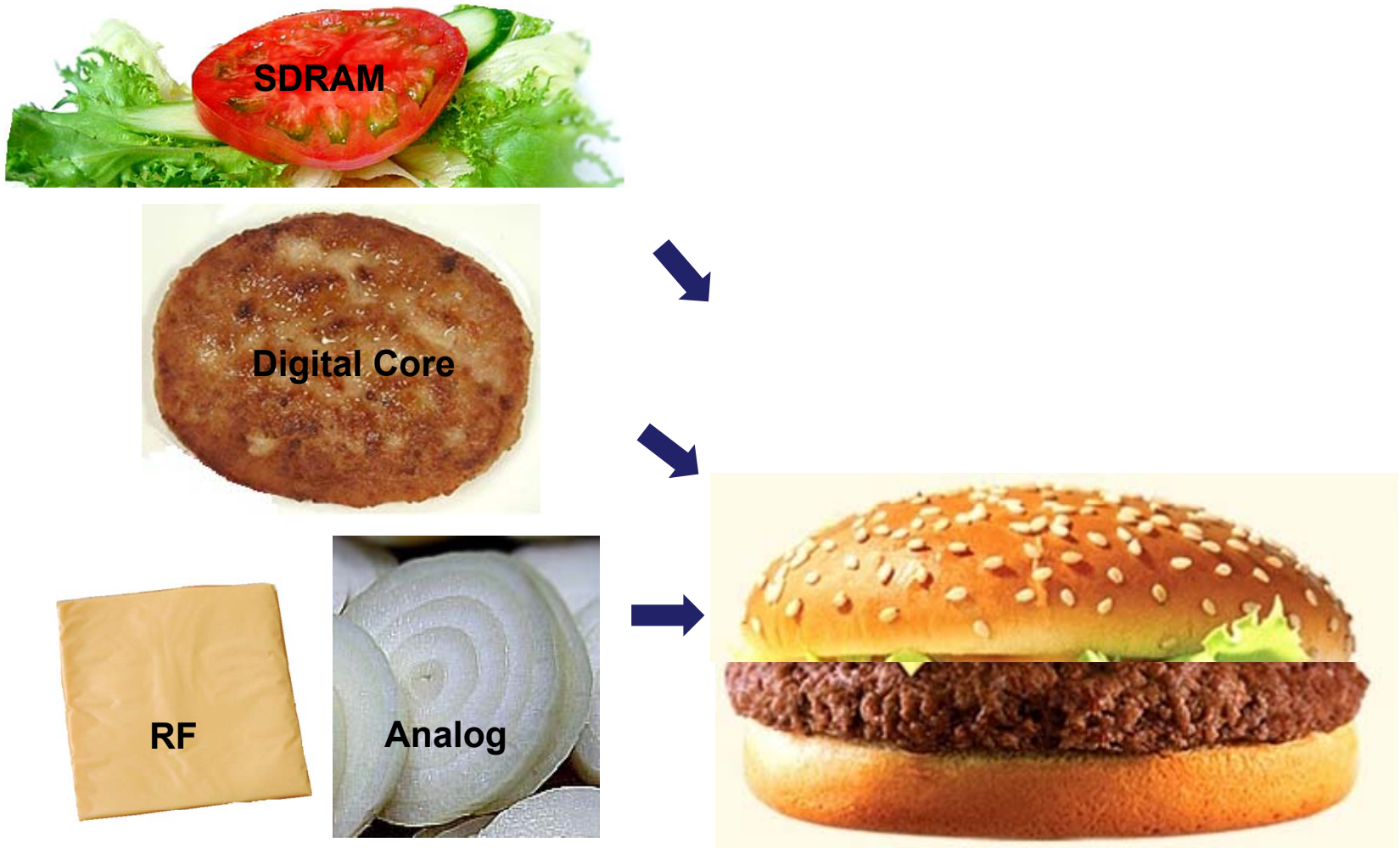

Sky Lounge
Apartment
Medical care center
Restaurant
Fitness & Spa
Parking



16GB Samsung NAND Flash, 8Gbx16



3D Hamburger



Expected Market of 3D IC

- **Market Driving Forces of 3D IC**

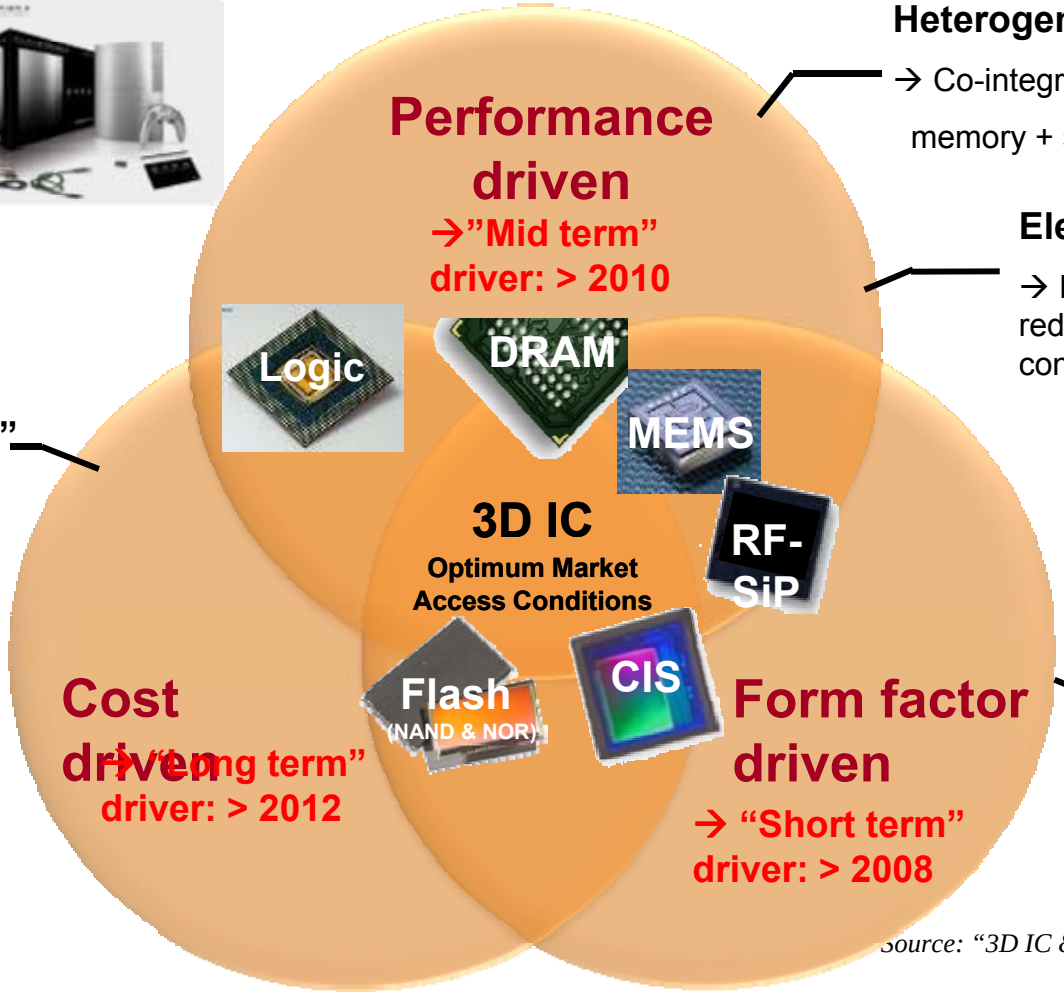
"More than Moore"
Heterogeneous integration

→ Co-integration of RF + logic + memory + sensors in a reduced space

Electrical performance

→ Interconnect speed and reduced parasitic power consumption

3D vs. "More Moore"
→ Can 3D be cheaper than going to the next lithography node?

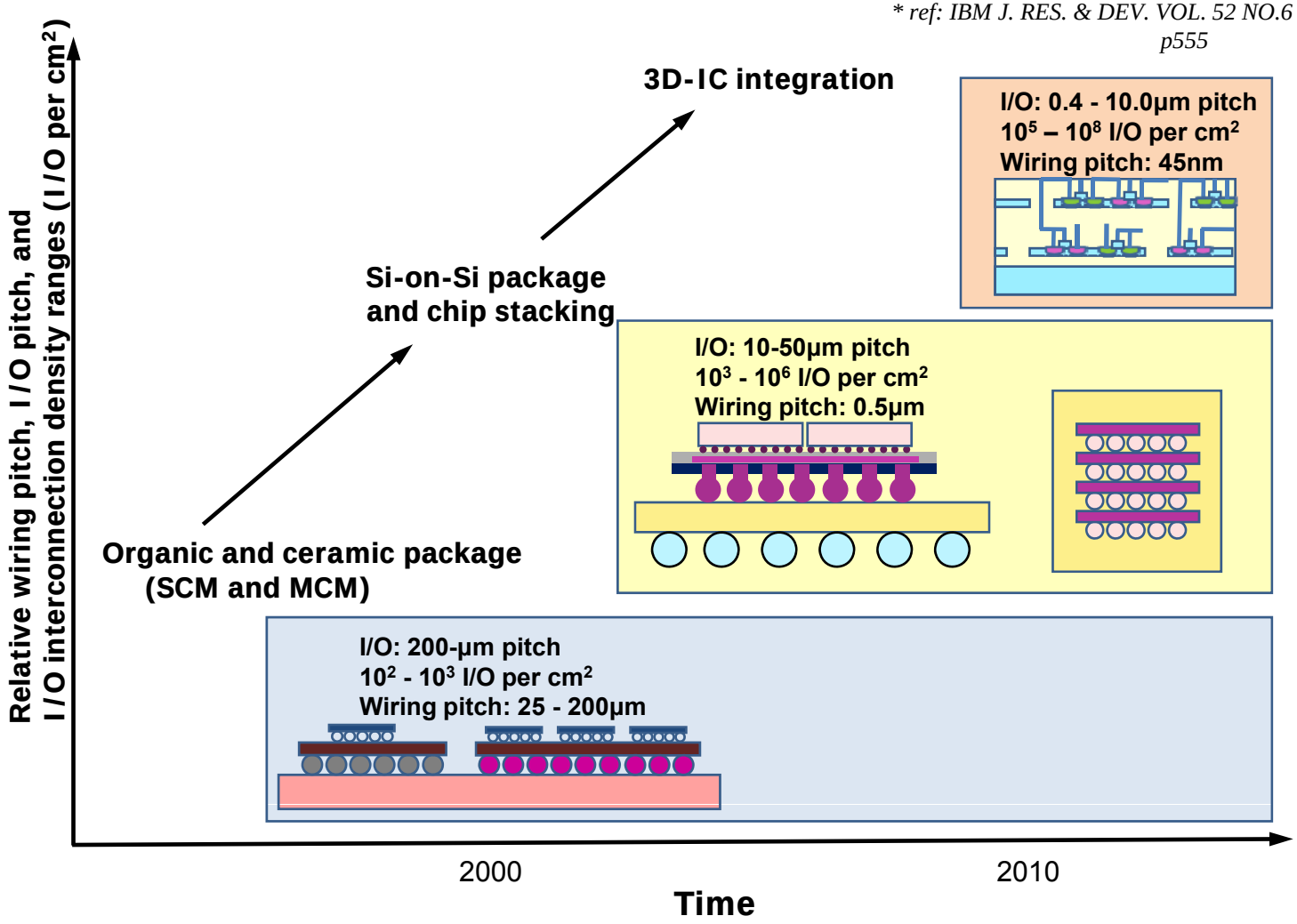


Density
→ Achieving the highest capacity / volume ratio

Source: "3D IC & TSV Report", Yole Development

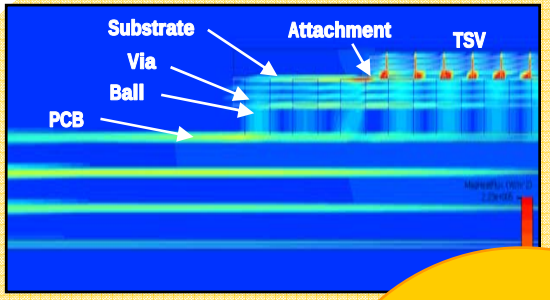
Technology Trend of 3D IC

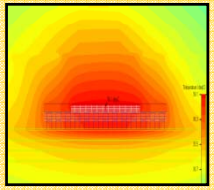
** ref: IBM J. RES. & DEV. VOL. 52 NO.6 NOVEMBER 2008, p555*



Relative comparison of I/O densities for 3D silicon, 3D die stacking, and silicon packaging, for both ceramic and organic packaging

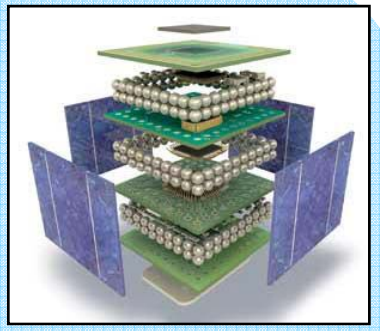
Core Technologies of 3D IC





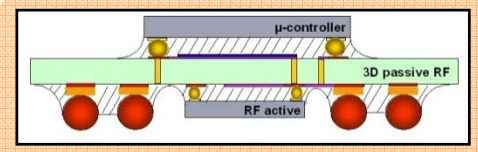
3D Thermal & Reliability Analysis And Design Methodologies

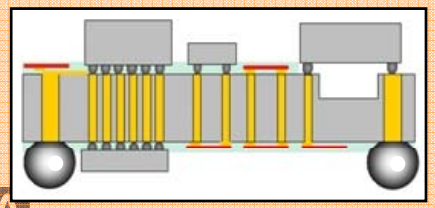
Unified Design/CAD Environment and Test



Chip & SoC Architecture and Design Methodologies

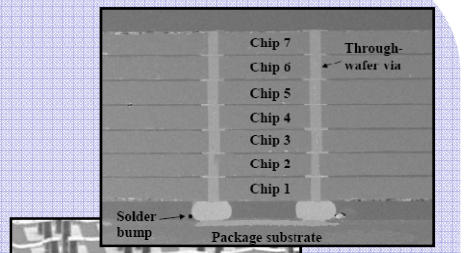
3D IC

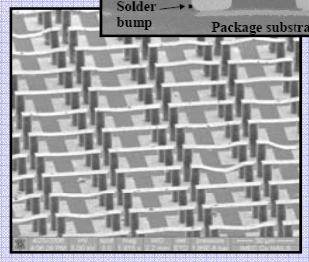




Low Cost Interposer Process and Design Technology

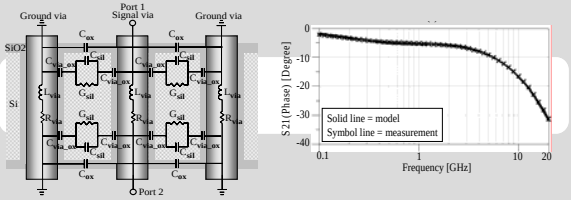
Chip-to-Wafer Stacking & Bonding, TSV Technology





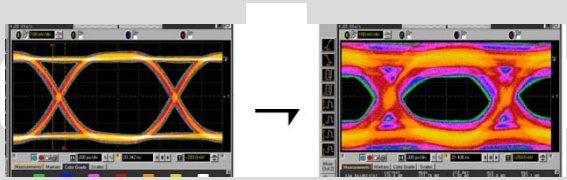
Signal Integrity Design Issues in 3D IC

Signal Integrity I: Loading Effect & Reflection



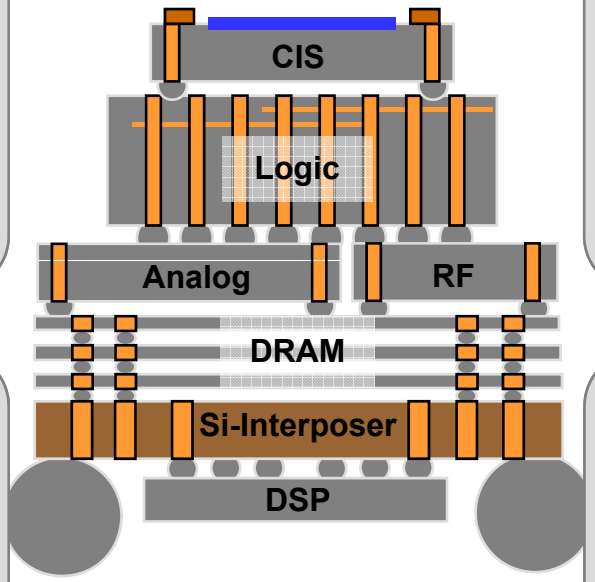
- Limitation of High Speed Signaling by Capacitive Loading
- Impedance Mismatching, Reflection

Signal Integrity II: Crosstalk & Jitter

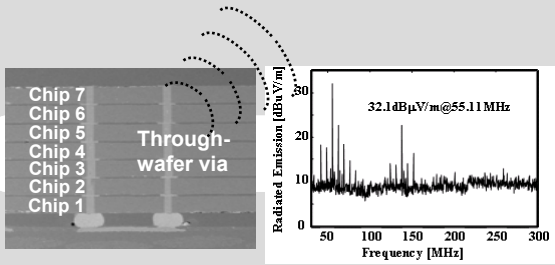


- Crosstalk Between TSVs
- Die-to-Die Vertical Coupling
- Jitter by Inter-Symbol-Interference

3D IC using TSV (Through Silicon Via)

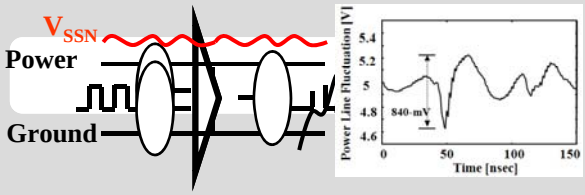


EMI



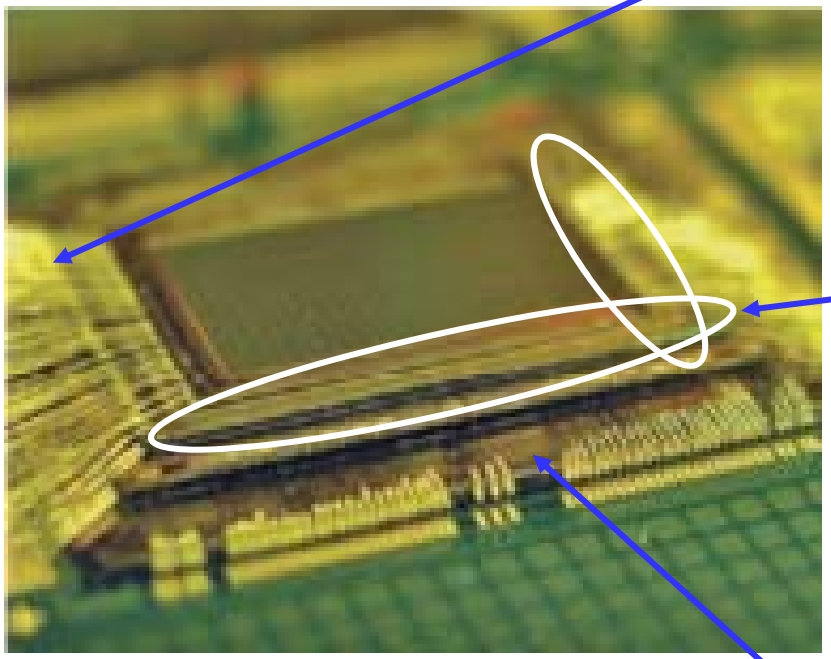
- Vertical Die-to-Die EMI Coupling
- RF Sensitivity Reduction by EMI
- EM Radiation Increase

Power Integrity



- Simultaneous Switching Noise caused by Insufficient Power
- High freq Noise Coupling & Transfer

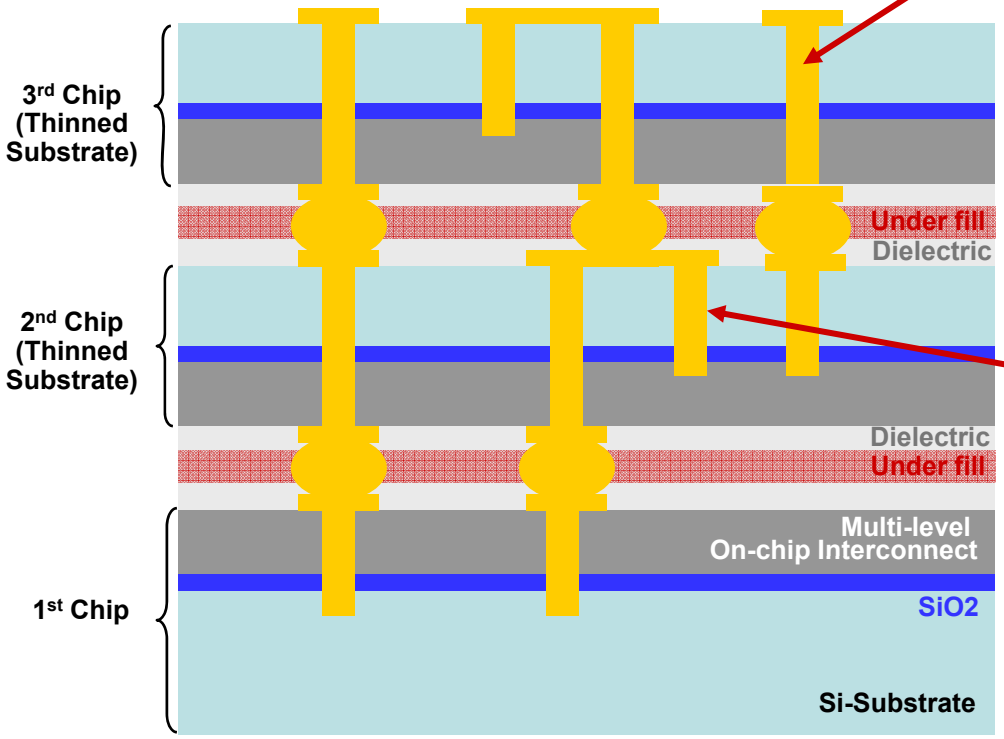
Disadvantages of Wire Bonding Stacked Chip Package



3D Stacked Chip Package with Wire Bonding

- **Long Interconnection**
  - → Long RC Delays
  - → High Impedance for Power Distribution Network
  - → High Power Consumption
  - → Poor Heat Dissipation (Thick Substrate)
- **Bonding Wire located in Chip Perimeter**
  - → Low Density Chip Wiring
  - → Limited Number of I/O
  - → Limited I/O Pitch
  - → Large Area Package
- **Complex Interposer**
  - → Long Redistribution Interconnection
  - → Bonding Wire located in Interposer Periphery

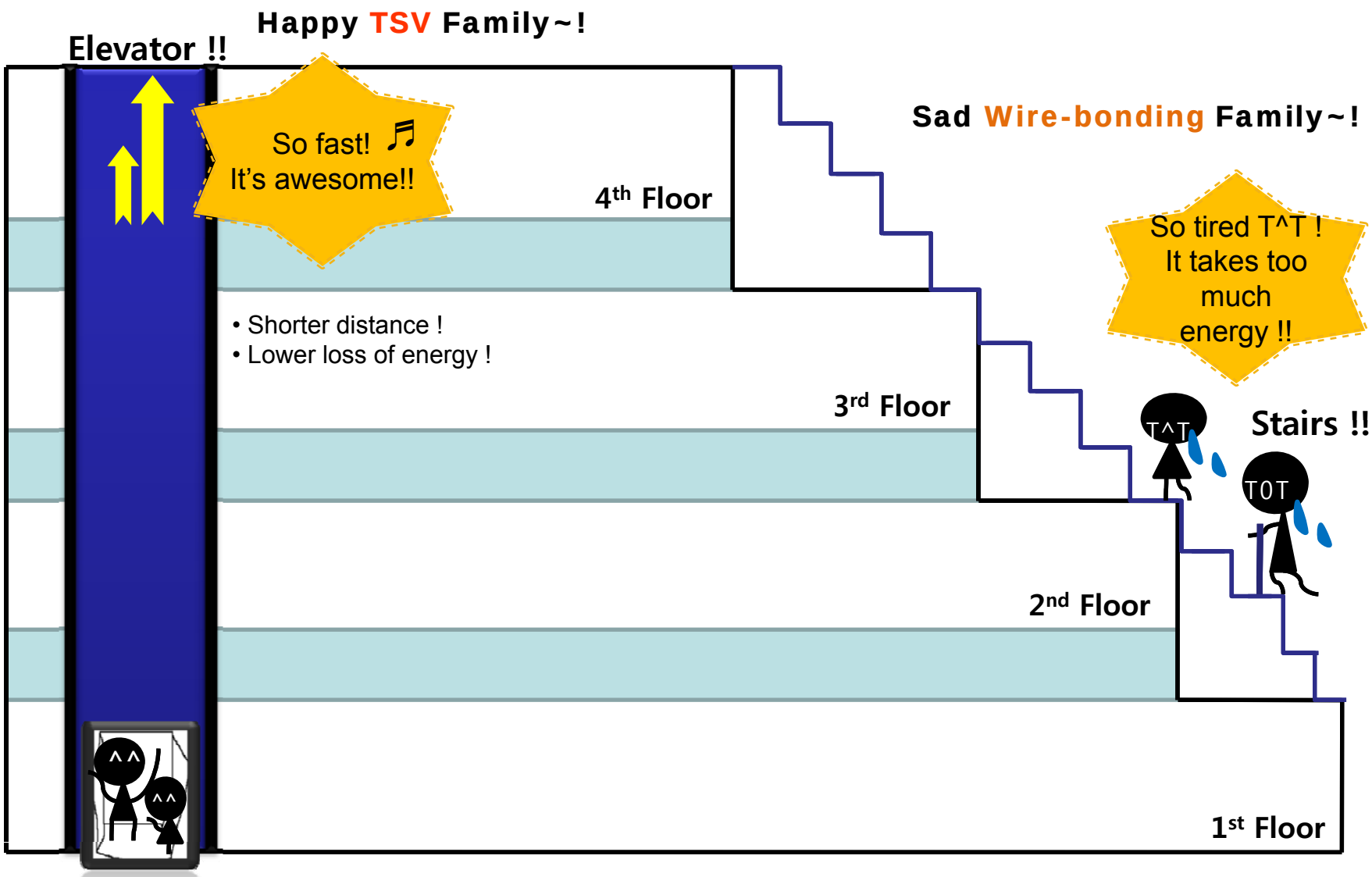
Key Technology : TSV (Through Silicon Via)



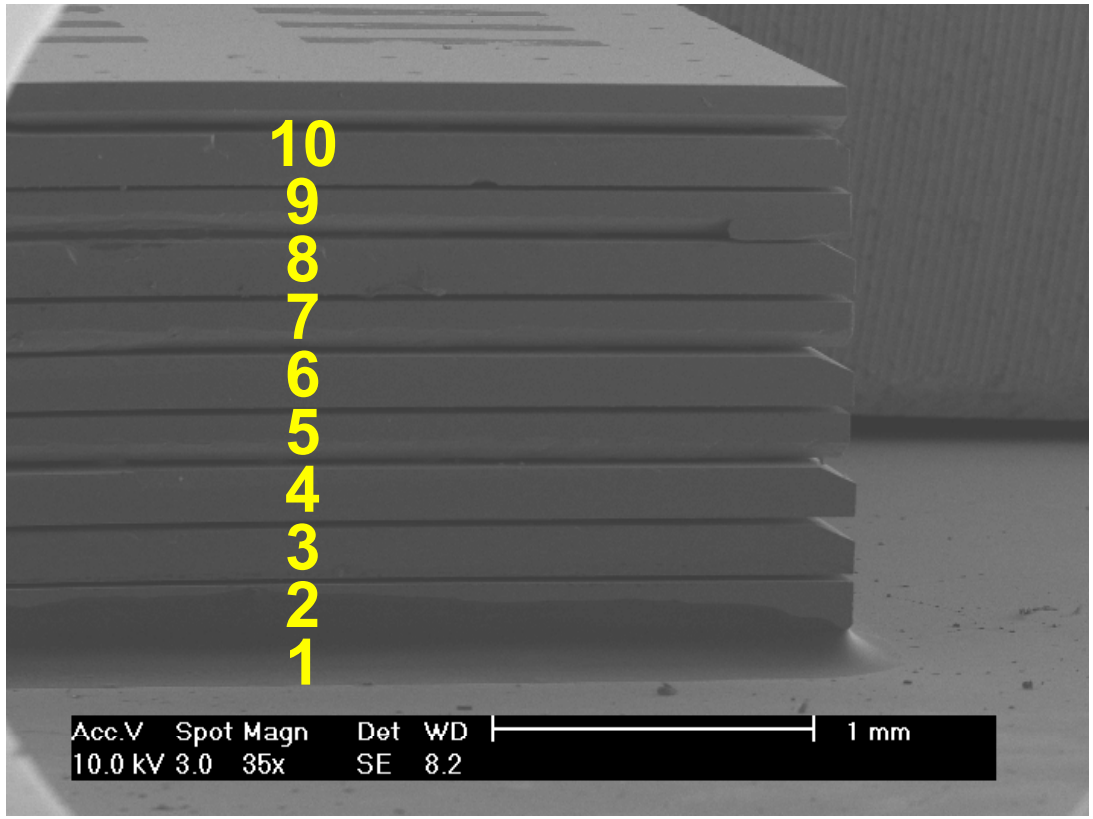
3D TSV Stacked IC

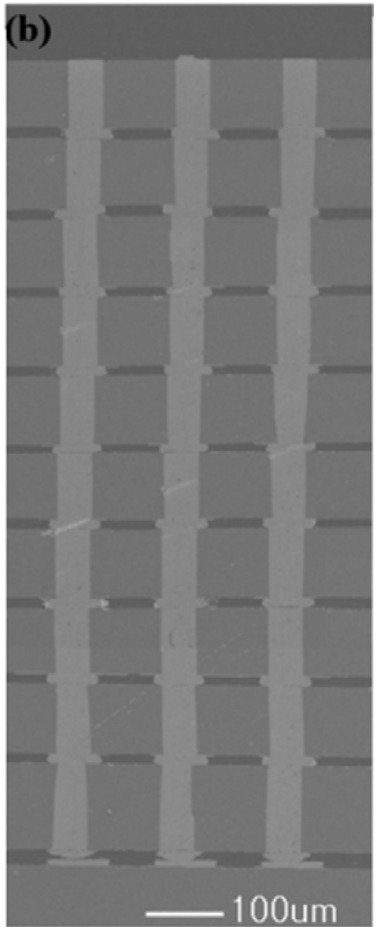
- **Short Interconnection**
  - → Reduced RC Delays
  - → Low Impedance for Power Distribution Network
  - → Low Power Consumption
  - → Heat Dissipation Through Via
- **No Space Limitation for Interconnection**
  - → High Density Chip Wiring
  - → No Limitation of I/O Number
  - → No Limitation of I/O Pitch
  - → Small Area Package

★ Why does TSV Family happy ^^ ?



10 chip stacked Package by KAIST





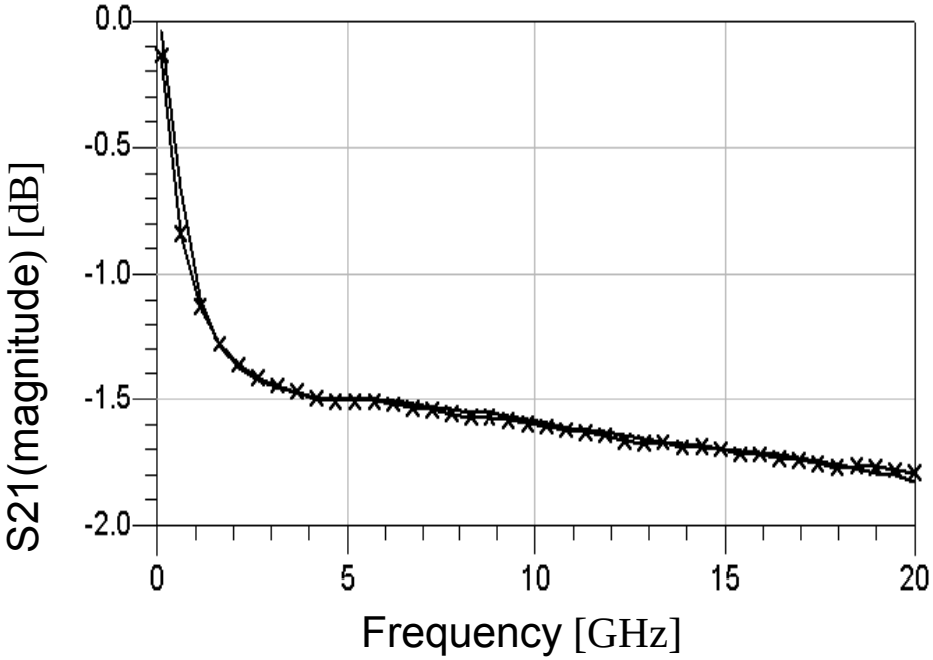
55 μm TSV diameter

150 μm Pitch

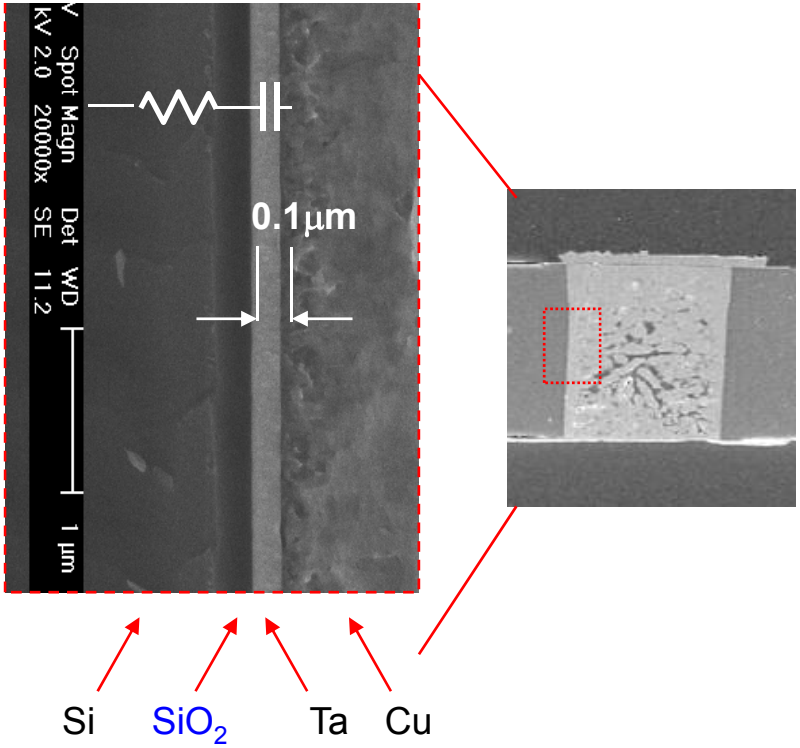
Background(1): High-frequency Channel Loss in TSV

-Significant high-frequency signal loss occur at Signal Transmission Through TSV

-The signal loss through TSV is caused by substrate leakage and coupling



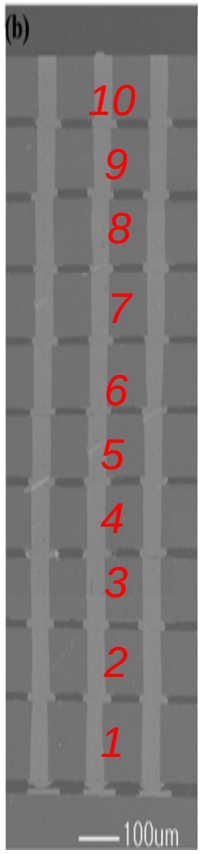
Magnitude of S21

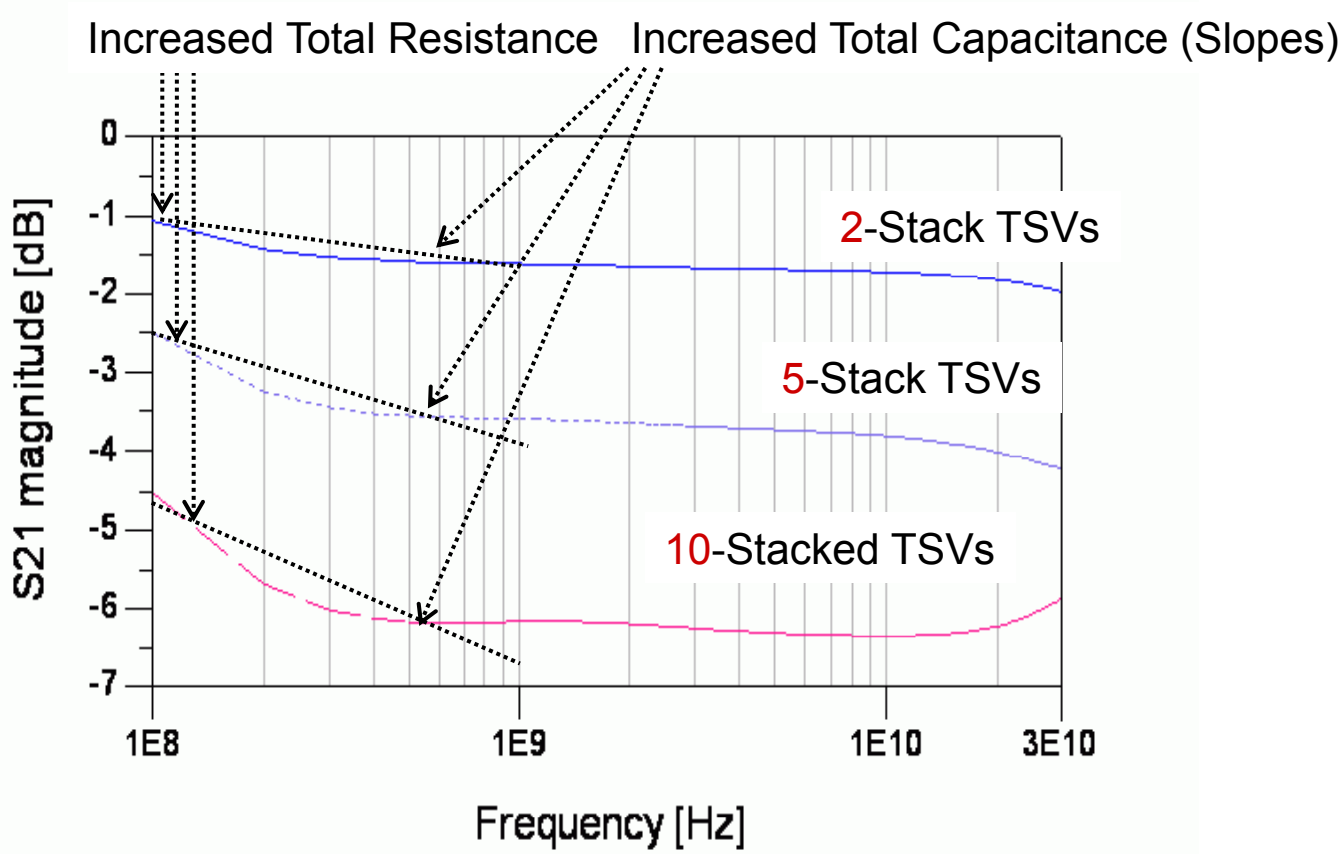


Close up of through wafer via

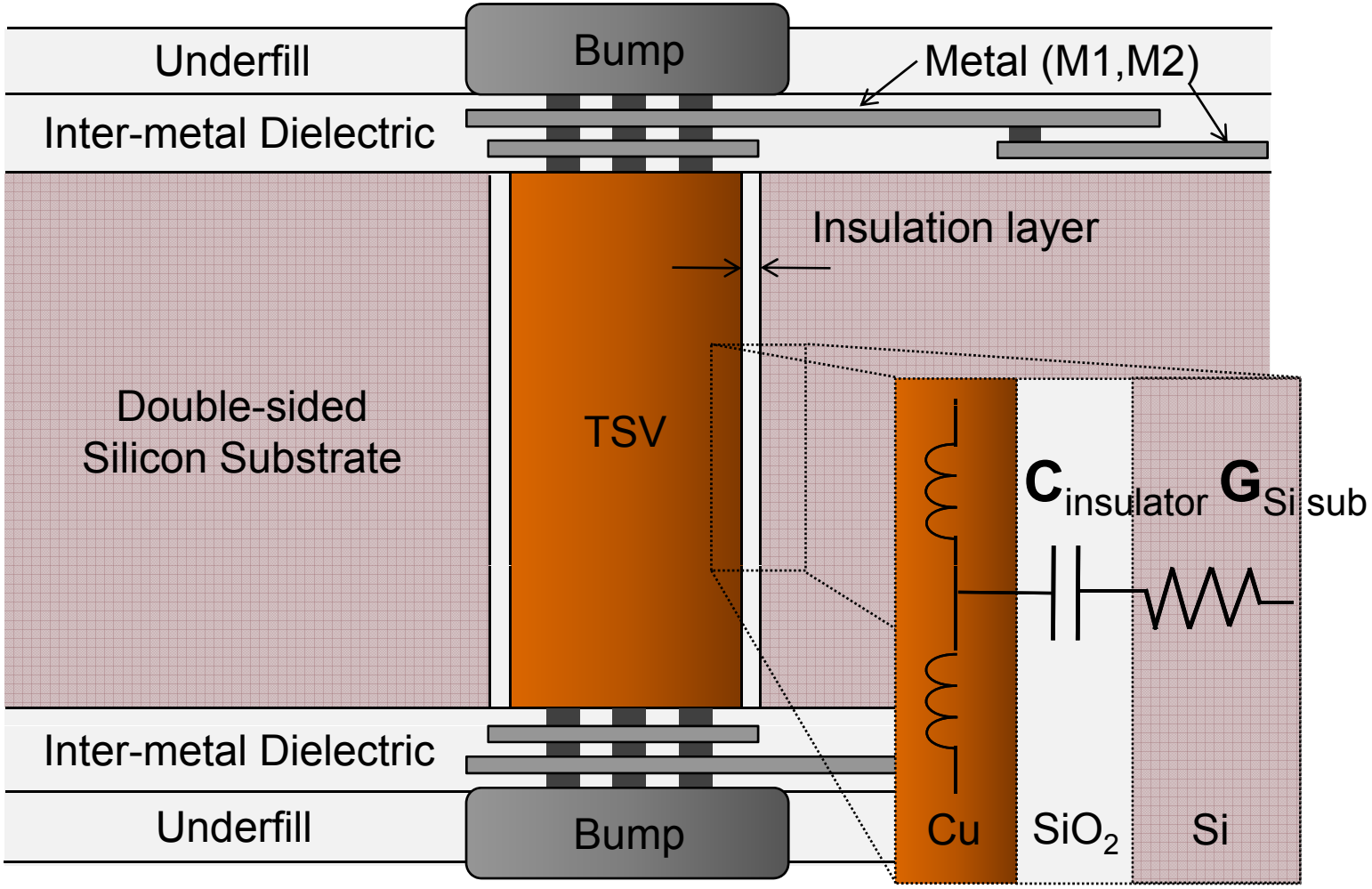
Background(2): Increased Channel Loss in Multi-Stack TSV

-Signal loss increases substantially with number of stacks/TSVs
-The signal loss through TSV is caused by substrate leakage and coupling

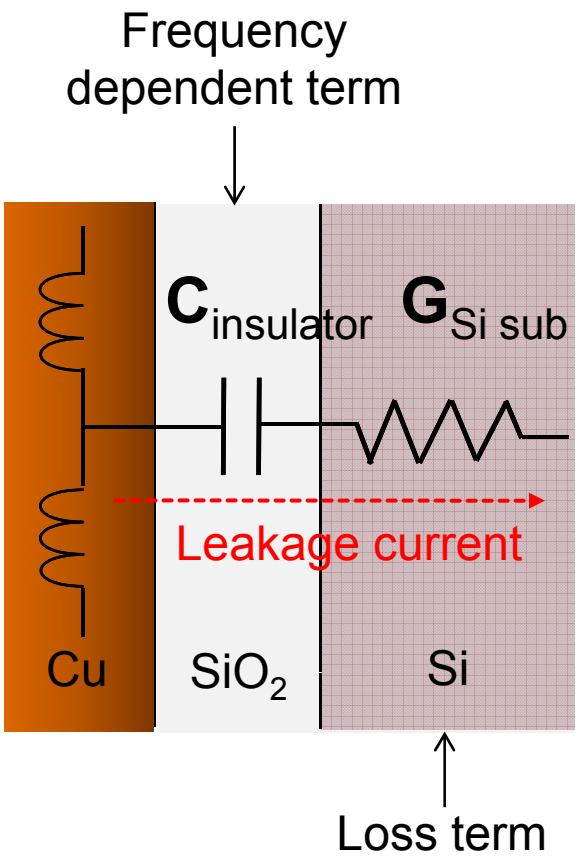


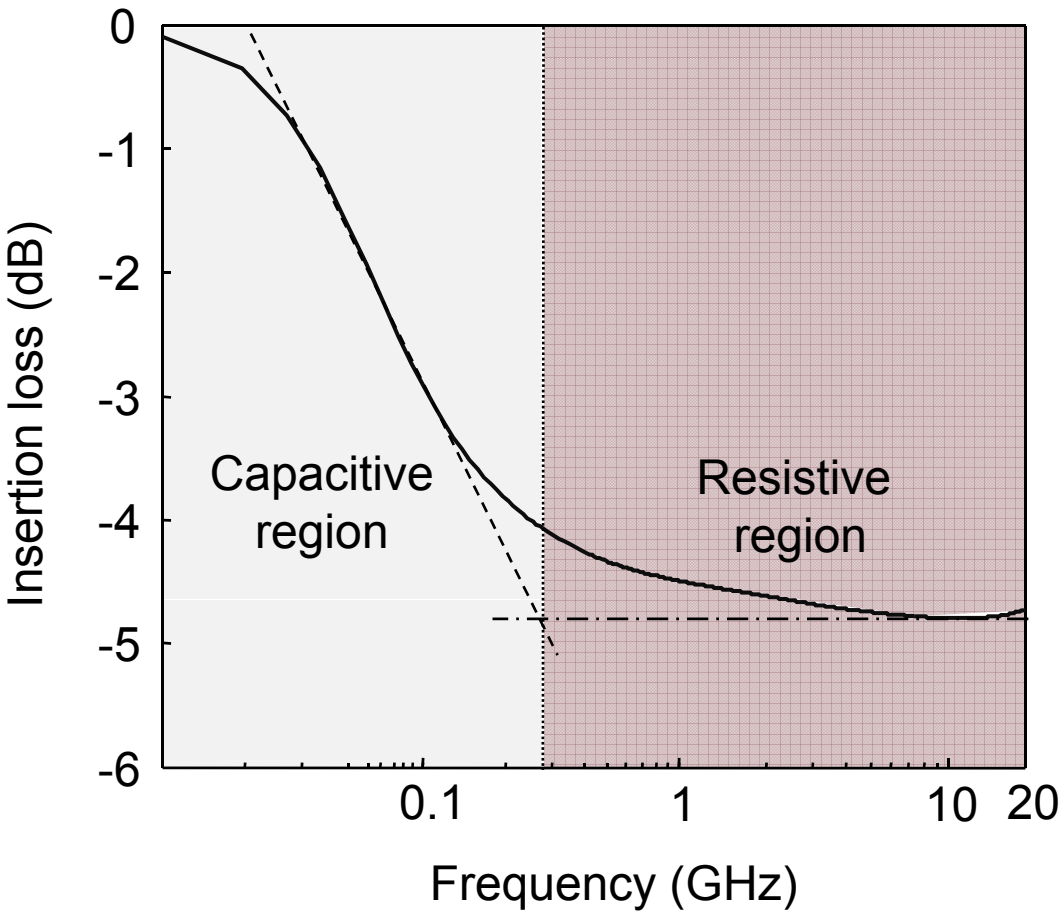


A Through Silicon Via Structure on Double-sided Silicon Substrate

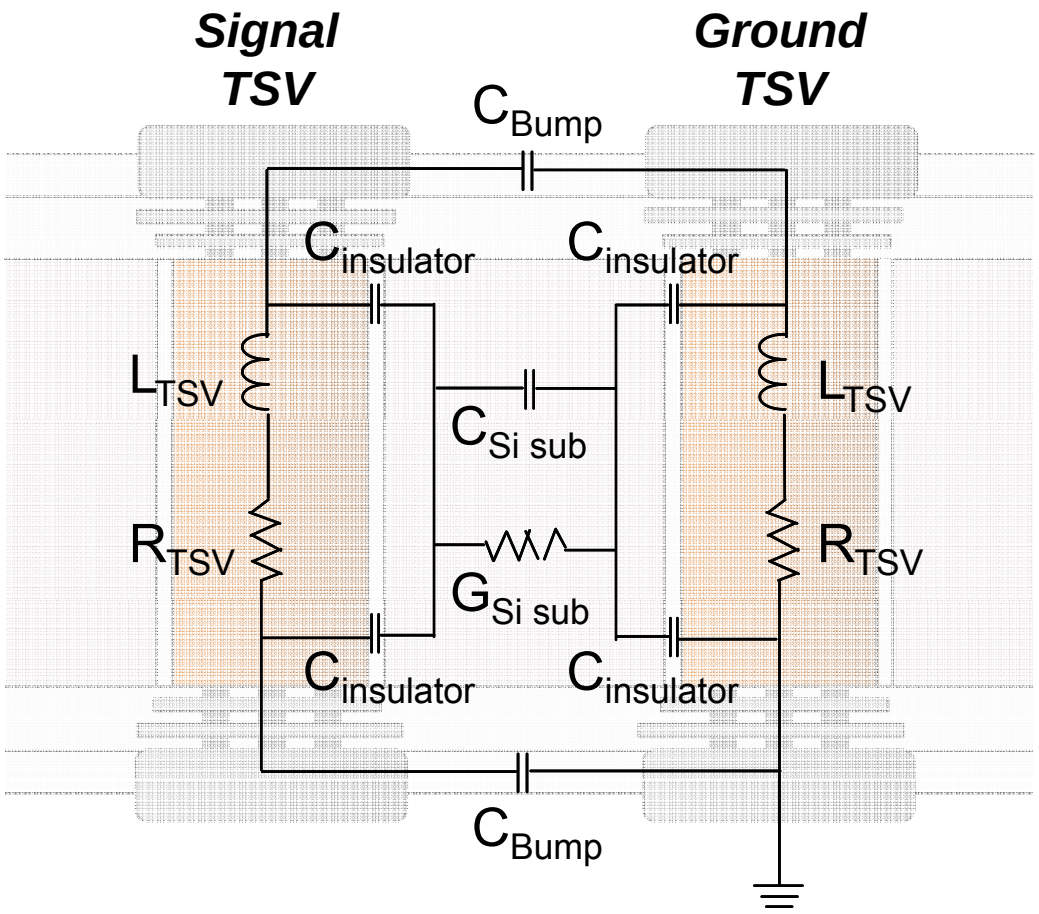


Frequency-dependent Loss of Through Silicon Via





Scalable Equivalent Circuit Model of a TSV



Structural Parameters

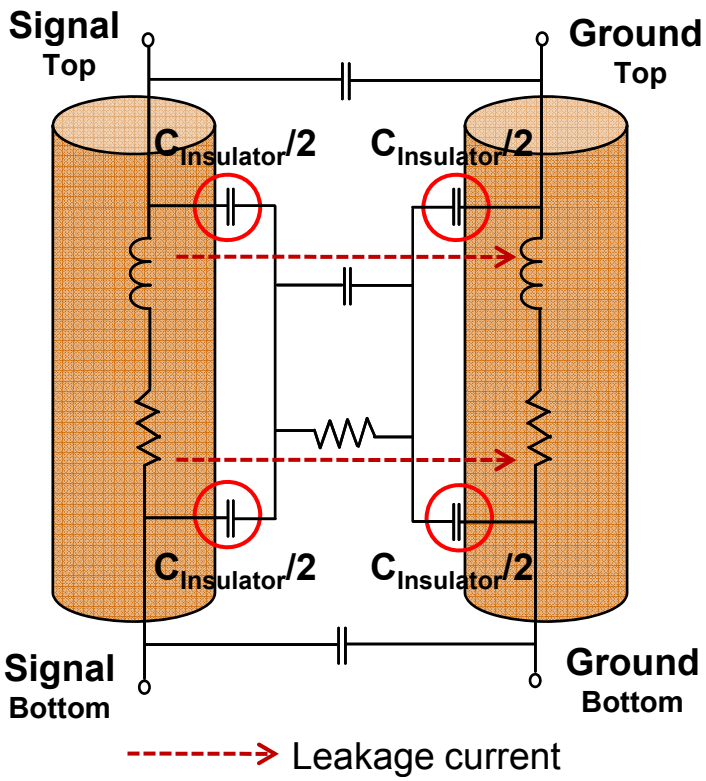
TSV diameter : d
TSV-to-TSV pitch : p
SiO2 thickness : t
Height : h
Bump diameter : D

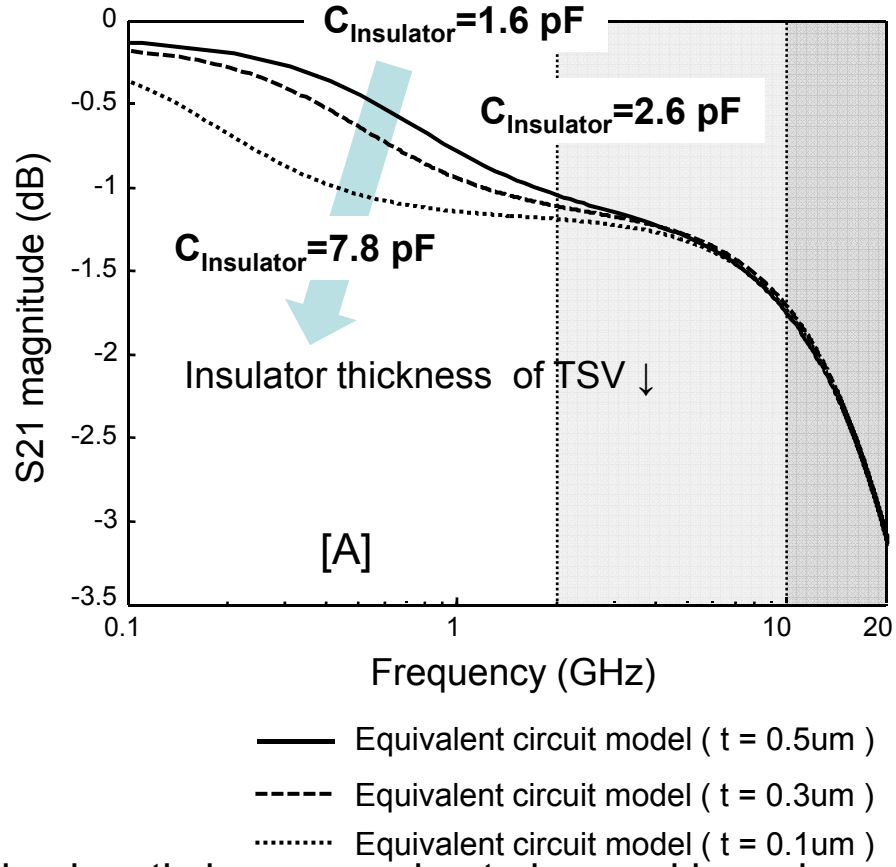
Equations

$C_{insulator}$ (d,h,t)
$C_{Si\ sub}$ (d,h,p,t)
C_{Bump} (p,D)
$G_{Si\ sub}$ (d,h,p,D)
R_{TSV} (d,h)
L_{TSV} (d,h,p)

Analysis of a TSV Channel with Insulator Thickness of TSV

- Insulator thickness of TSV (t)



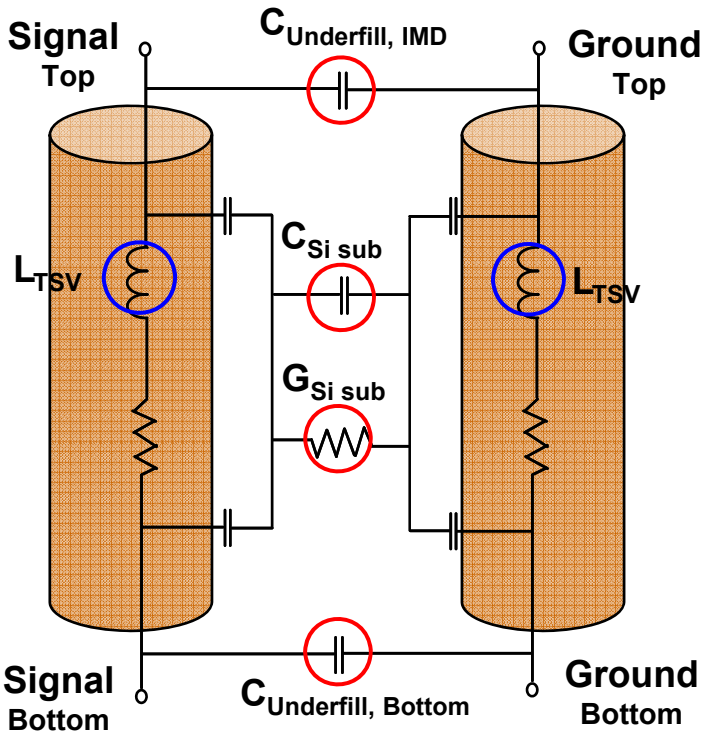


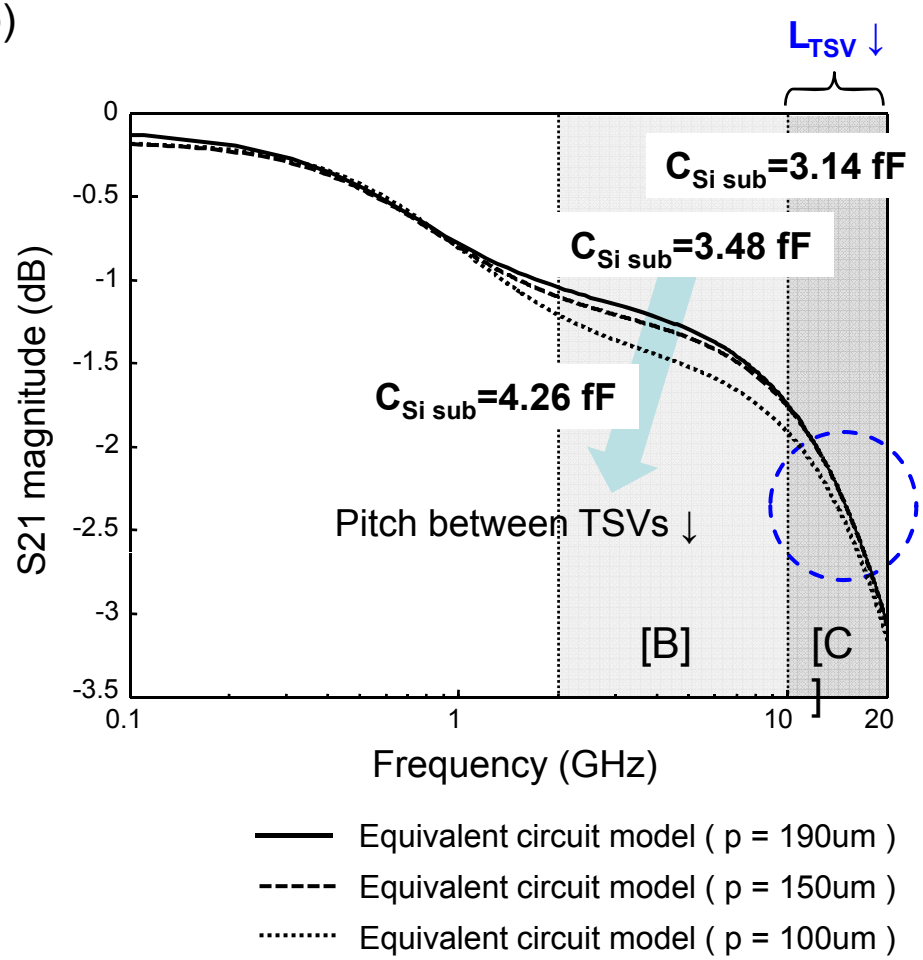
➔ Leakage through silicon substrate dominantly increases due to lowered impedance with increased $C_{insulator}$ in region [A].

➔ Insulator thickness dominantly affects frequency dependent loss of a TSV channel in region [A].

Analysis of a TSV Channel with Pitch between TSVs

- Pitch between Signal & Ground TSV (p)





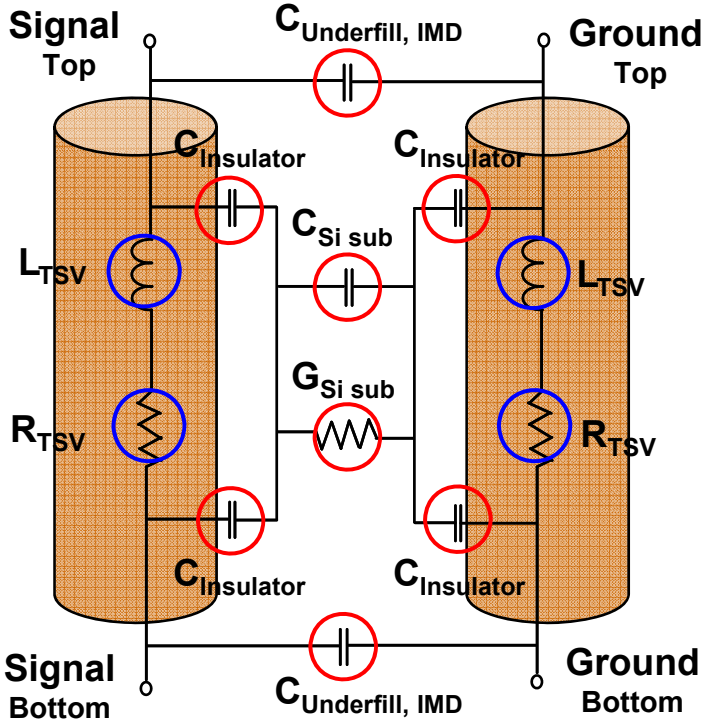
➔Due to relative small capacitance, pitch affects frequency dependent loss of a TSV channel from region [B].

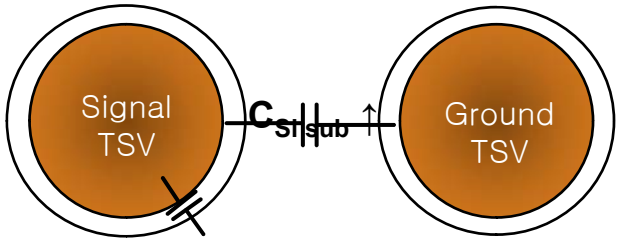
➔ From region [C], inductance effect becomes dominant.

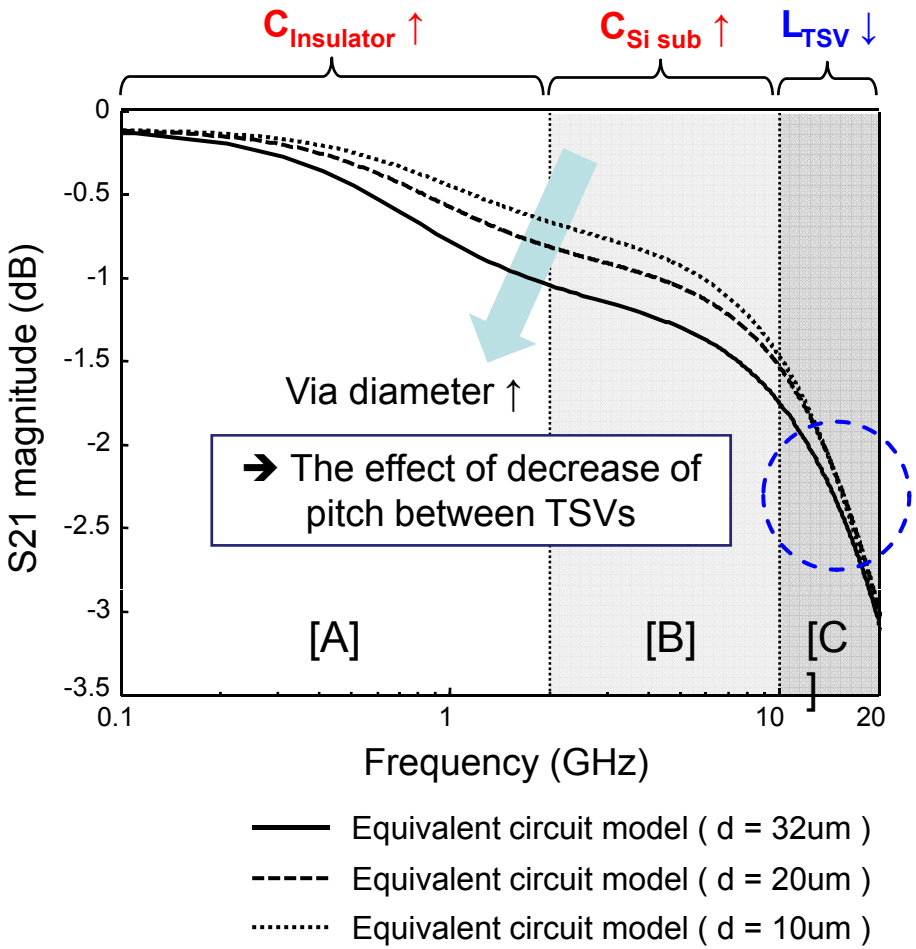
➔ Pitch dominantly affects frequency dependent loss of a TSV channel in region [B].

Analysis of a TSV Channel with TSV Diameter

- Via diameter of TSV (d)





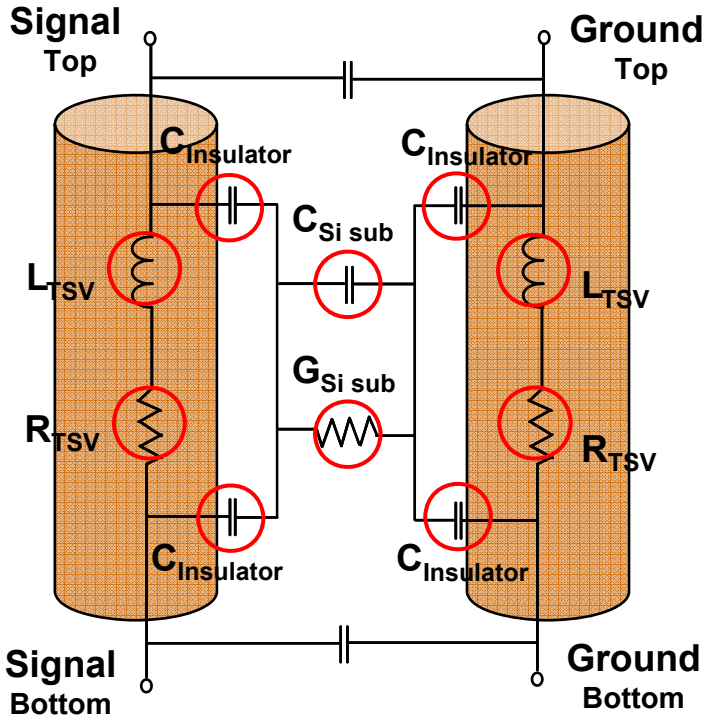


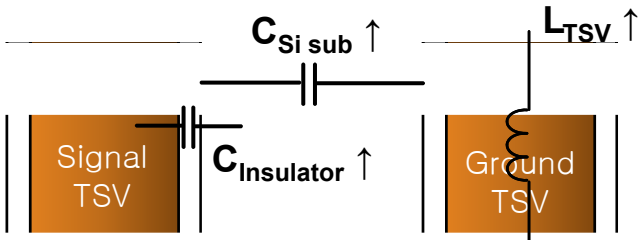
$C_{Insulator}$ ↑

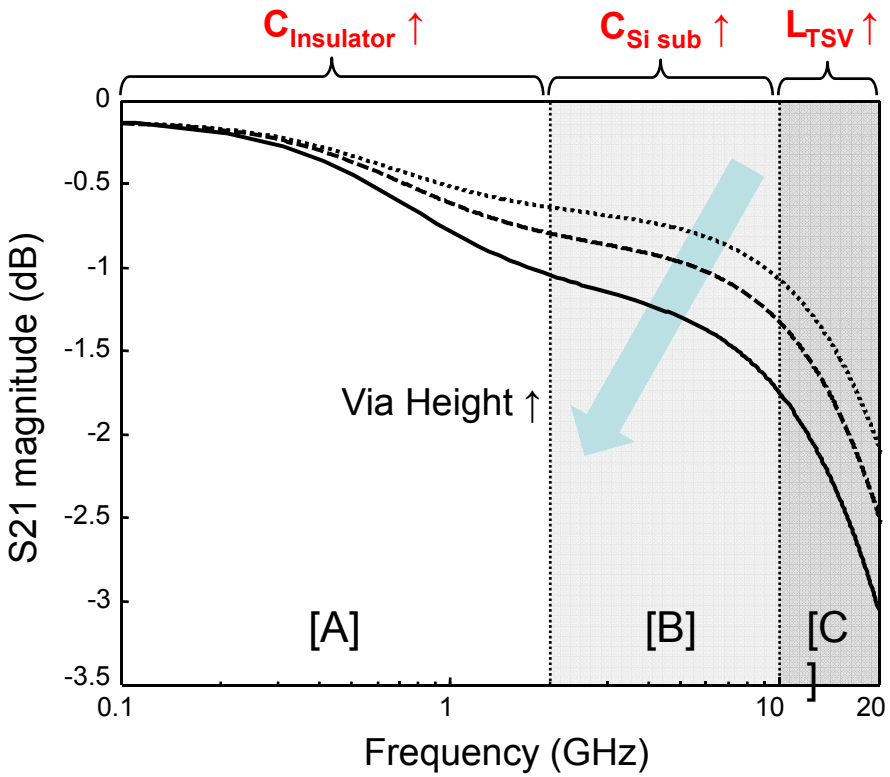
➔ Via diameter affects frequency dependent loss of a TSV channel, dominantly in region [A] and [B].

Analysis of a TSV Channel with Via Height of TSV

- Via height of TSV (h)







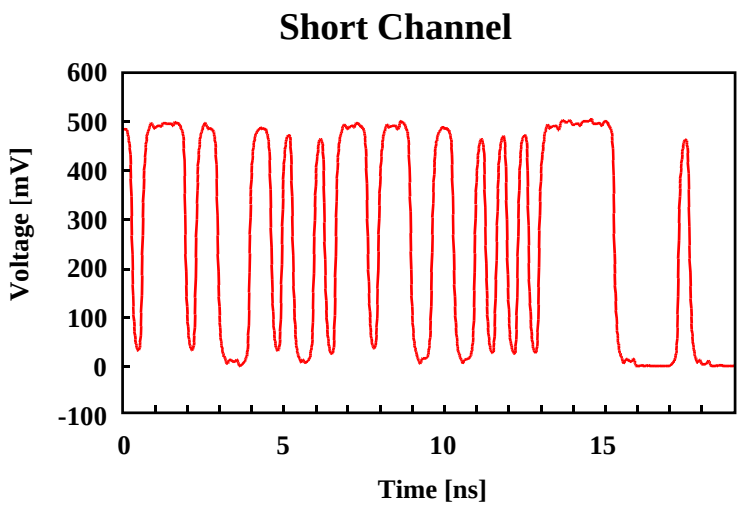
Equivalent circuit model (h = 110um)
Equivalent circuit model (h = 80um)
Equivalent circuit model (h = 50um)

➔ Via height affects frequency dependent loss of a TSV channel in all frequency ranges.

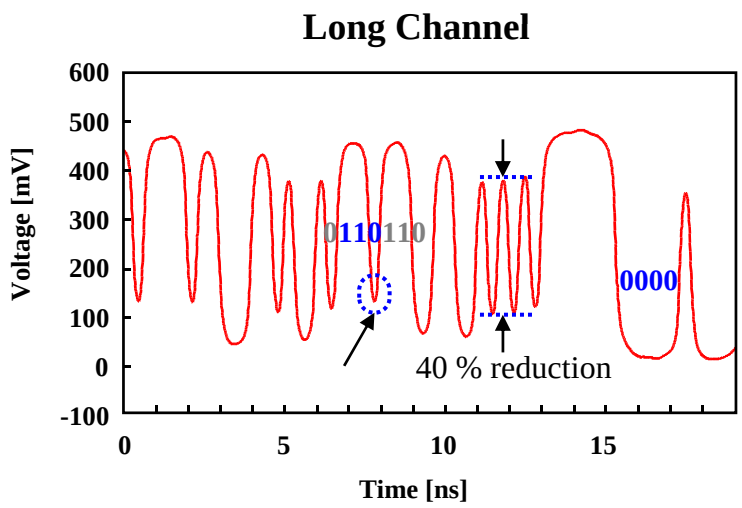
Inter-symbol Interference (ISI) by Channel Loss

- **Inter-symbol Interference is the interference between adjacent pulses of a data**

- The channel BW Limit degrades the signal quality
- It depends on line-length, data rate and sub. materials on PCB



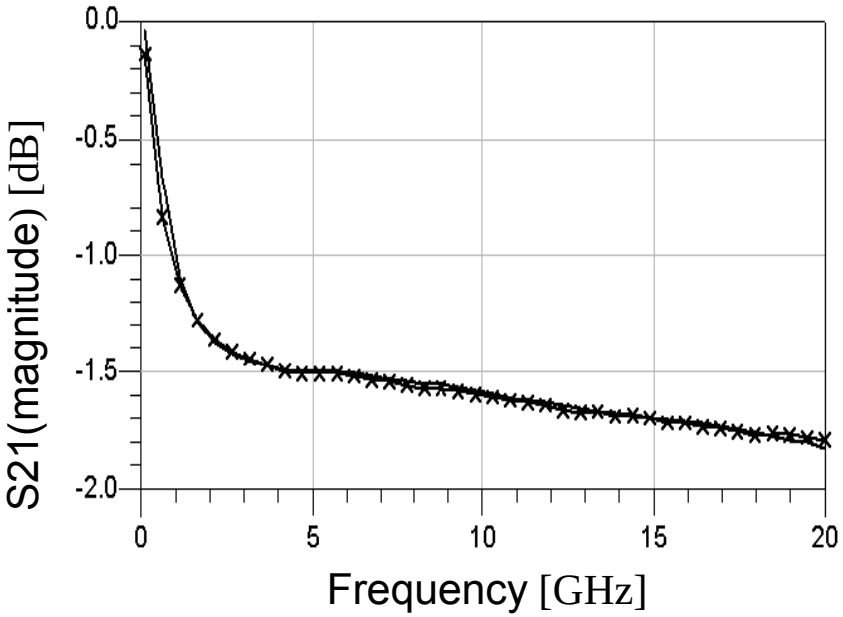
– **Channel Length = 10 cm**
– 3 Gbps
– FR4 (Loss Tangent = 0.03)

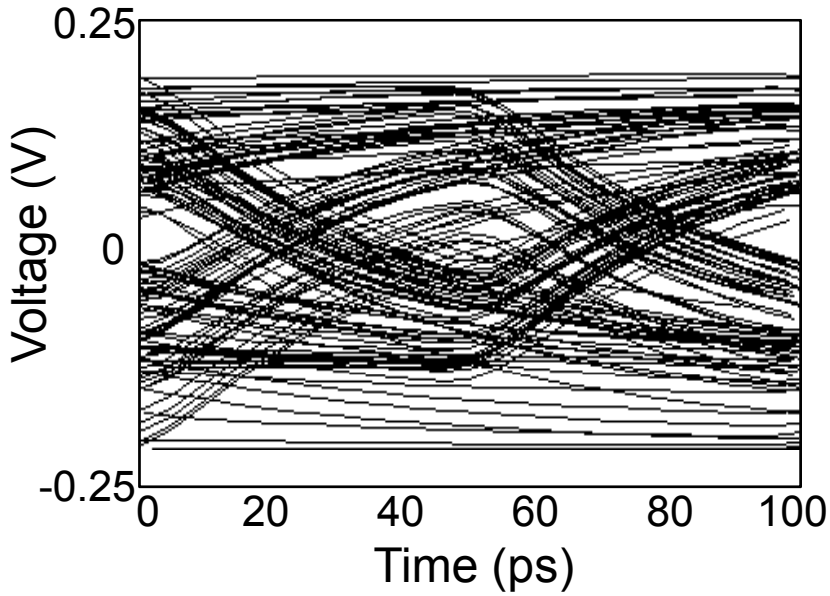


– **Channel Length = 40 cm**
– 3 Gbps
– FR4 (Loss Tangent = 0.03)

[ISI effect due to line-length]

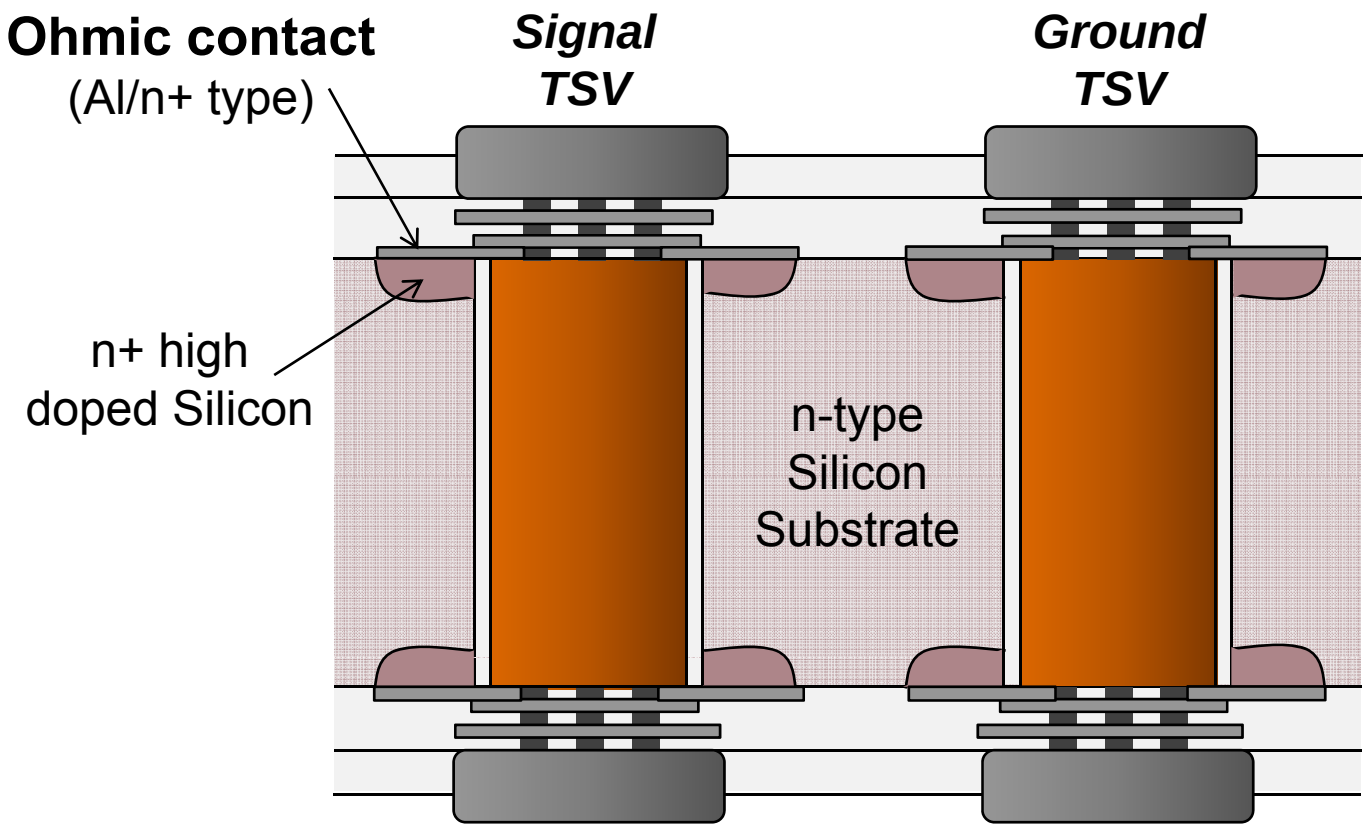
Inter-Symbol Interference at the TSV Equalizer





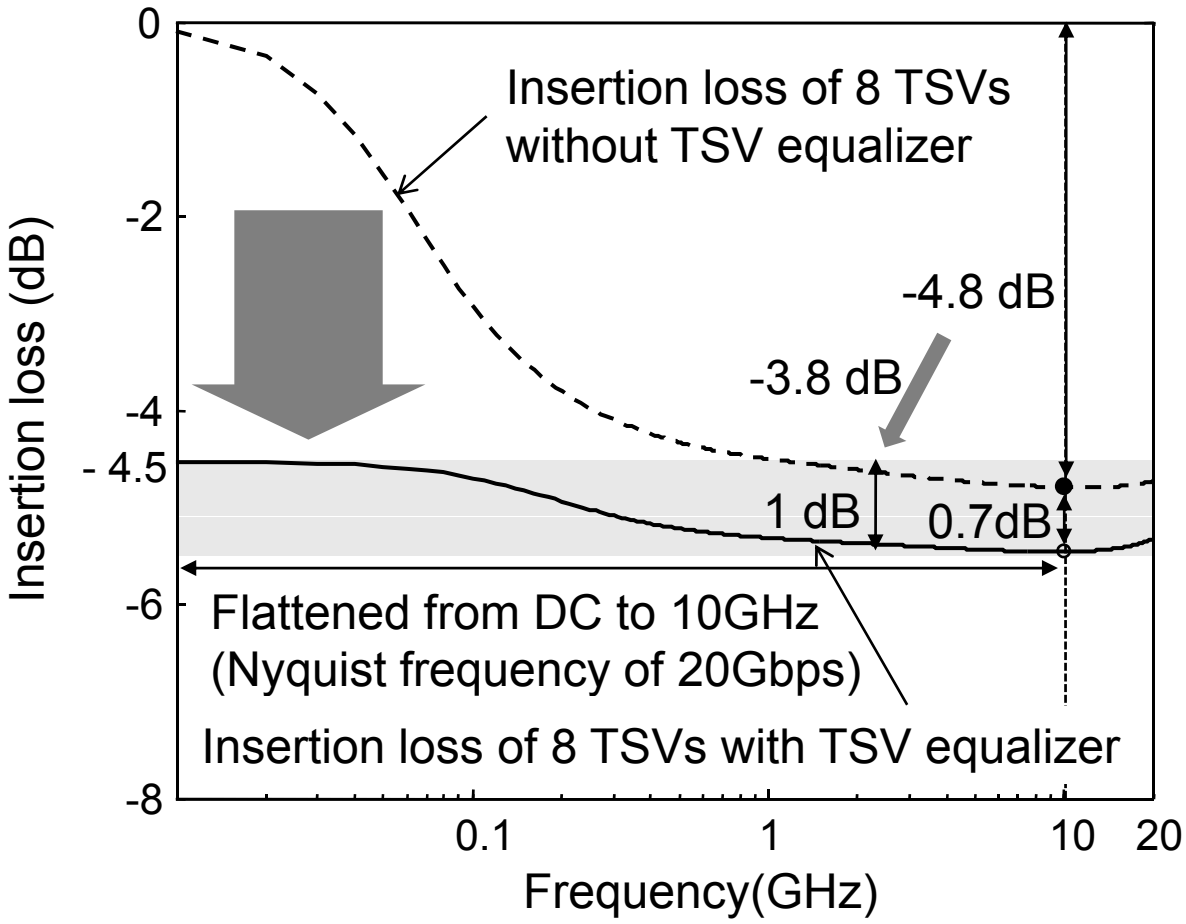
Magnitude of S21

The Proposed TSV Equalizer using an Ohmic Contact



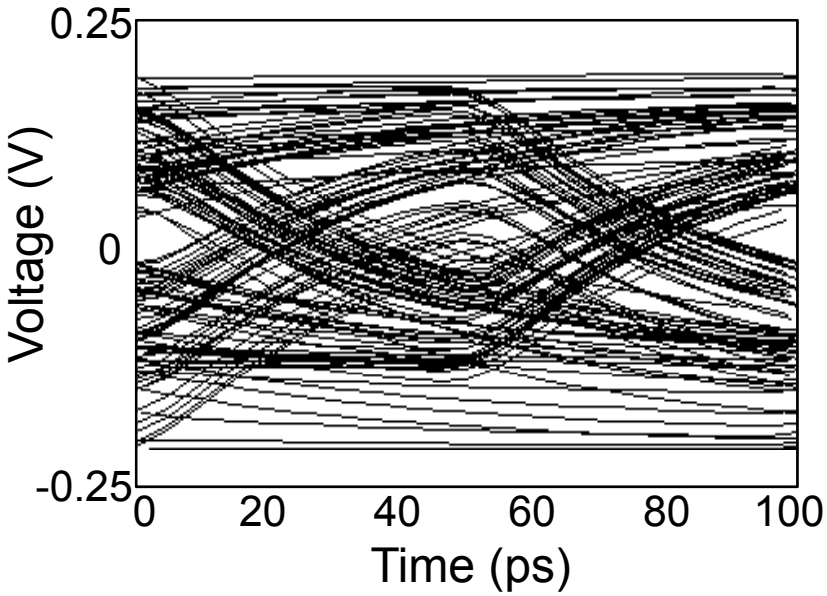
- We intentionally made leakage by using an **Ohmic contact** resulting in **DC attenuation** between signal and ground TSV.

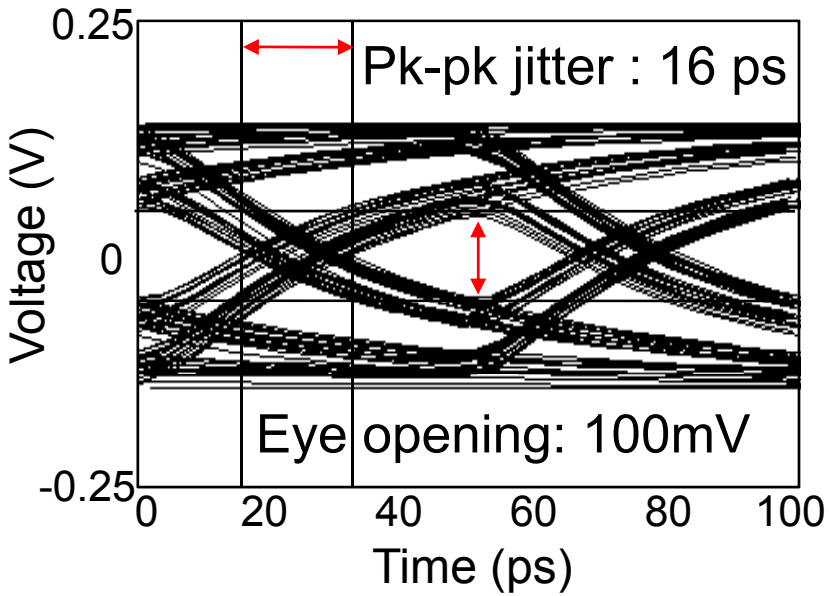
Frequency Domain Simulation-based Verification of the TSV Equalizer Performance



- We successfully flattened frequency dependent loss by 3.8 dB by using TSV Equalizer.

Time Domain Simulation-based Verification of the TSV Equalizer Performance

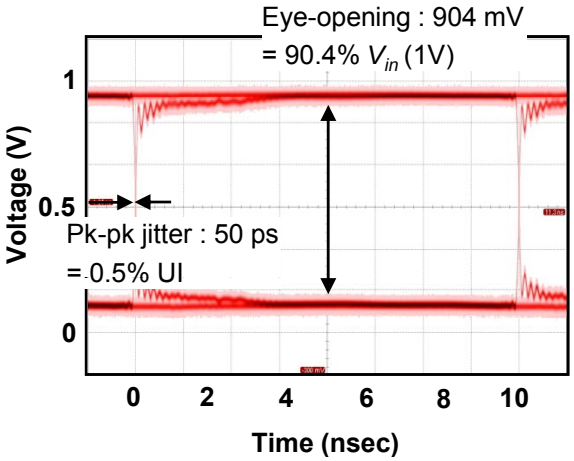


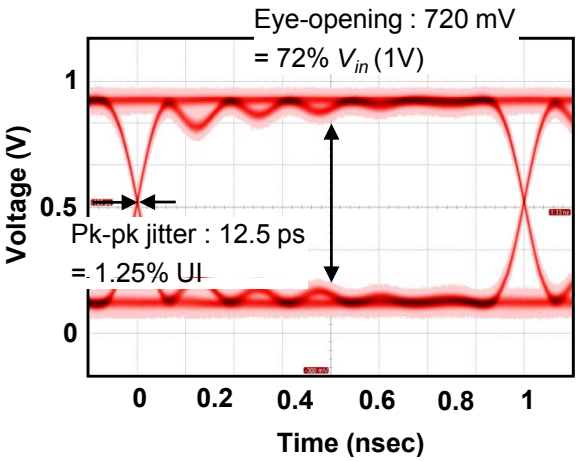


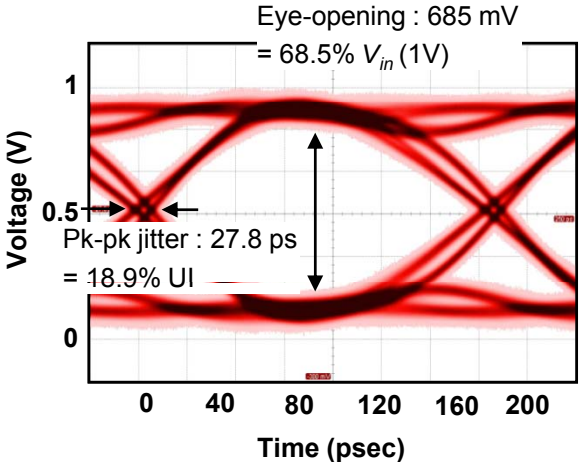
- We successfully achieved normalized pk-pk jitter and eye-opening, 32% and 20%, meanwhile the unequalized eye is completely closed.

Time-Domain Measurement Results

- **Measured Eye-diagrams of a TSV channel**





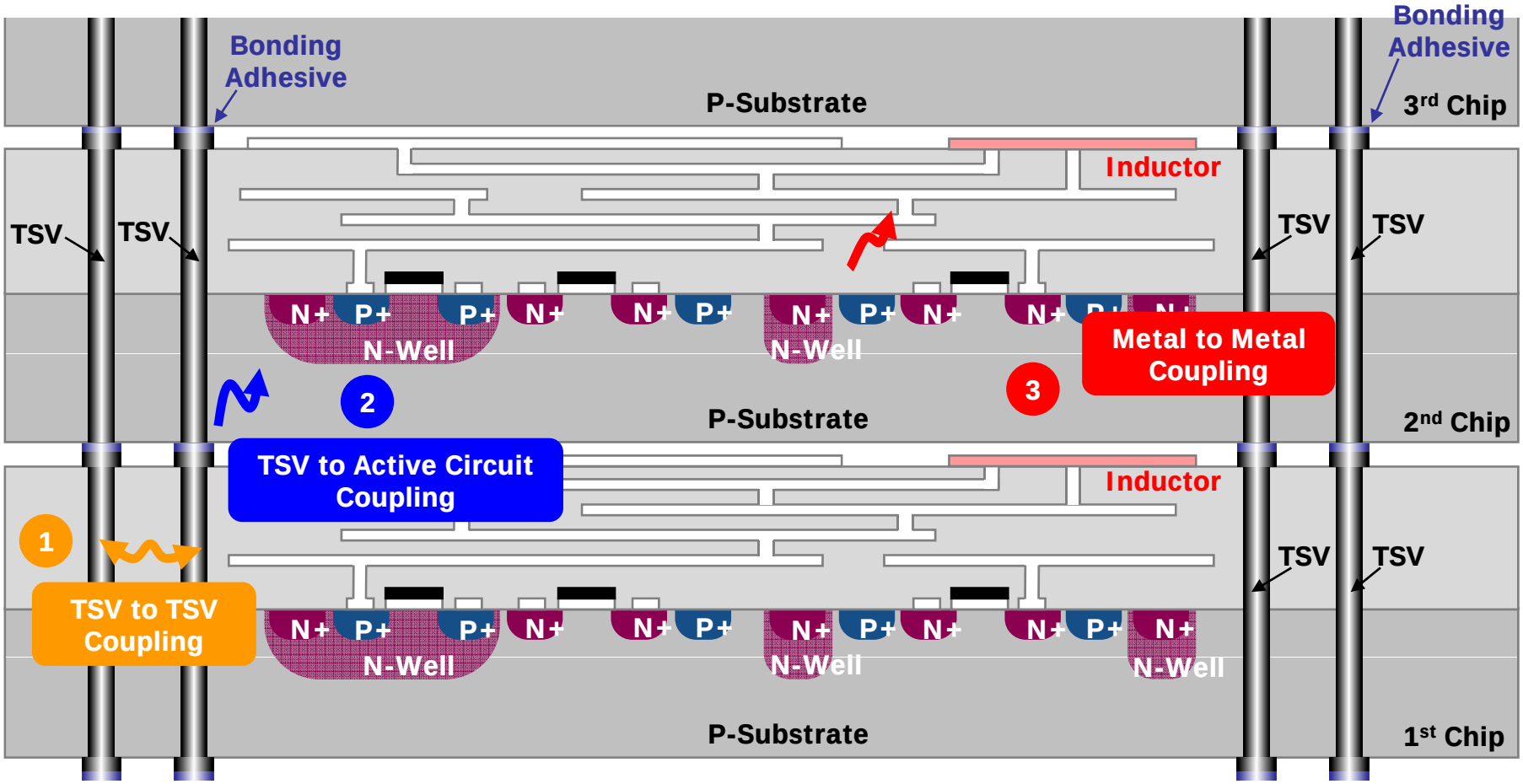


- Data rate : 100 Mb/s
- Data Pattern : PRBS 2^{11}-1,
- Source amplitude : 1 V

- Data rate : 1 Gb/s
- Data Pattern : PRBS 2^{11}-1,
- Source amplitude : 1 V

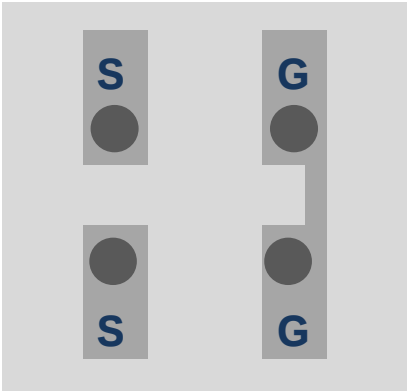
- Data rate : 5 Gb/s
- Data Pattern : PRBS 2^{11}-1,
- Source amplitude : 1 V

Coupling Issues in Stacked Dies using TSV

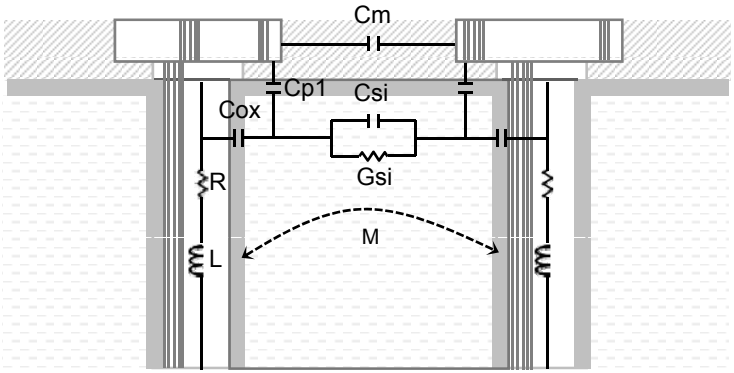


< CROSSSECTIONAL VIEW >

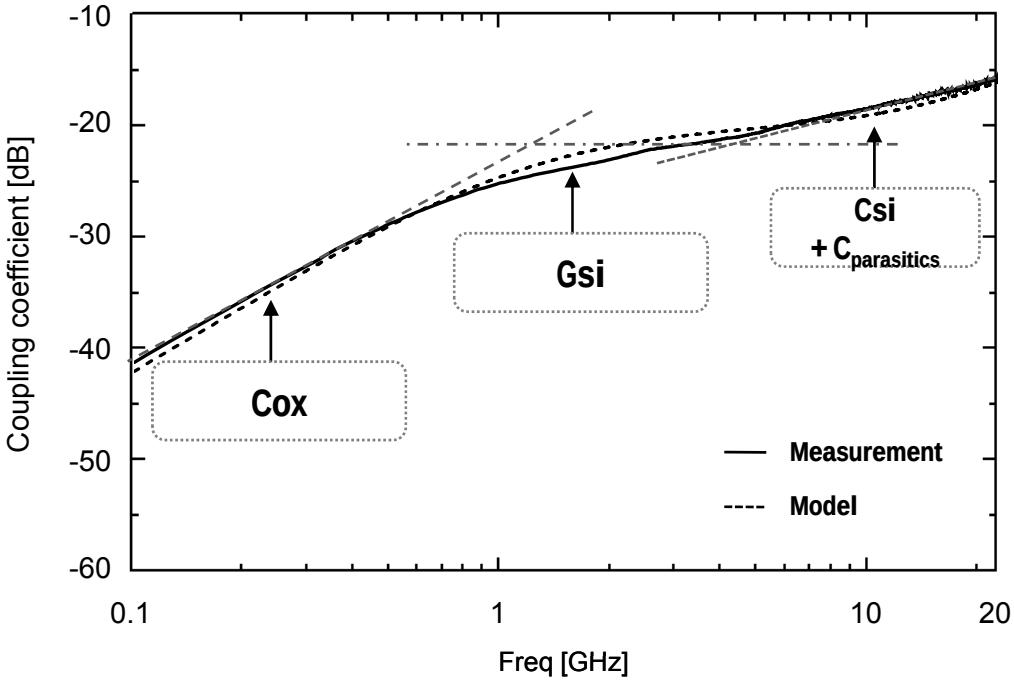
Measurement Result of Coupling between TSVs



< Top view>



< Equivalent circuit model of coupled TSV>

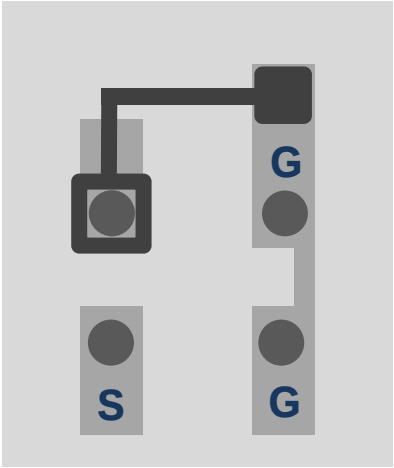


- **Analytic model of coupling between TSVs shows good agreement with measurement result**

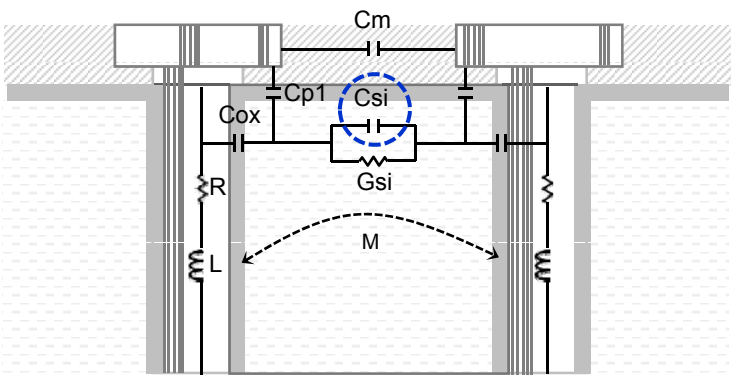
Shielding Methods for TSV Coupling

1) Re-design of TSV materials and dimensions
2) Separation
3) Guard Ring
4) GND Shield TSV
5) Metal Ring

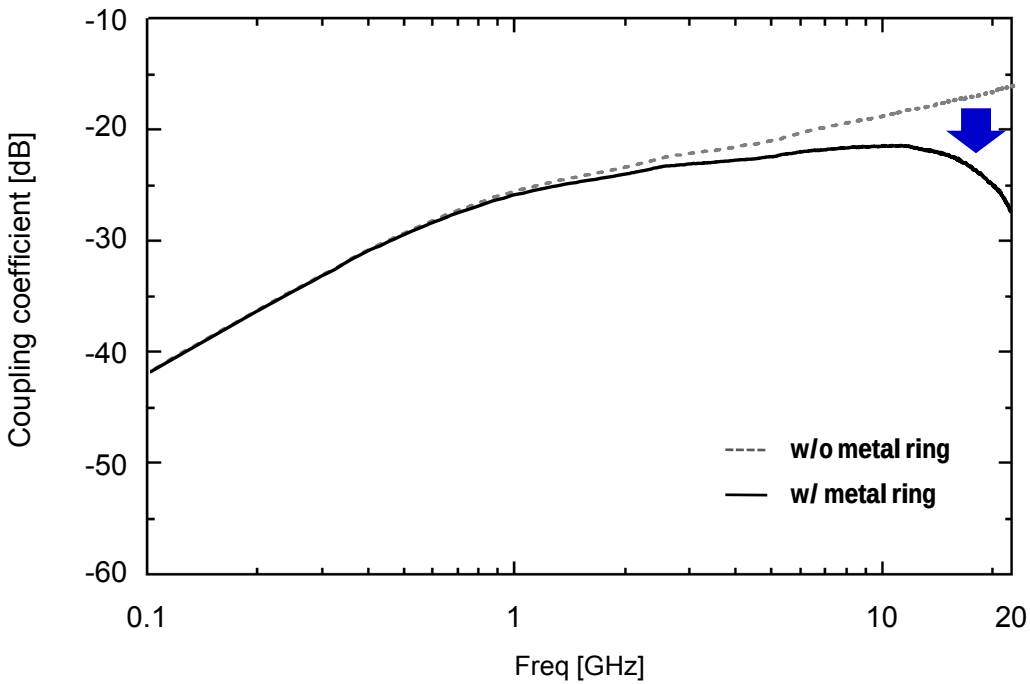
Shielding Effect Measurement – (1) Metal Ring



< Top view>

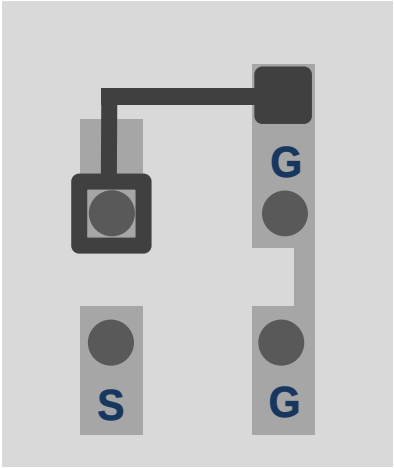


< Equivalent circuit model of coupled TSV>

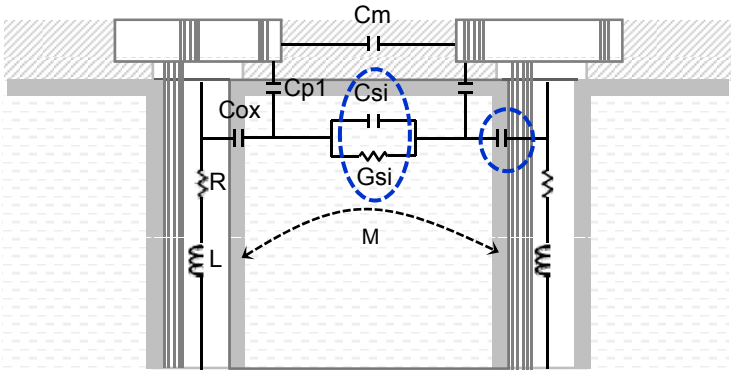


- **Metal ring has shielding effect only in high frequency because it blocks coupling in IMD layer**

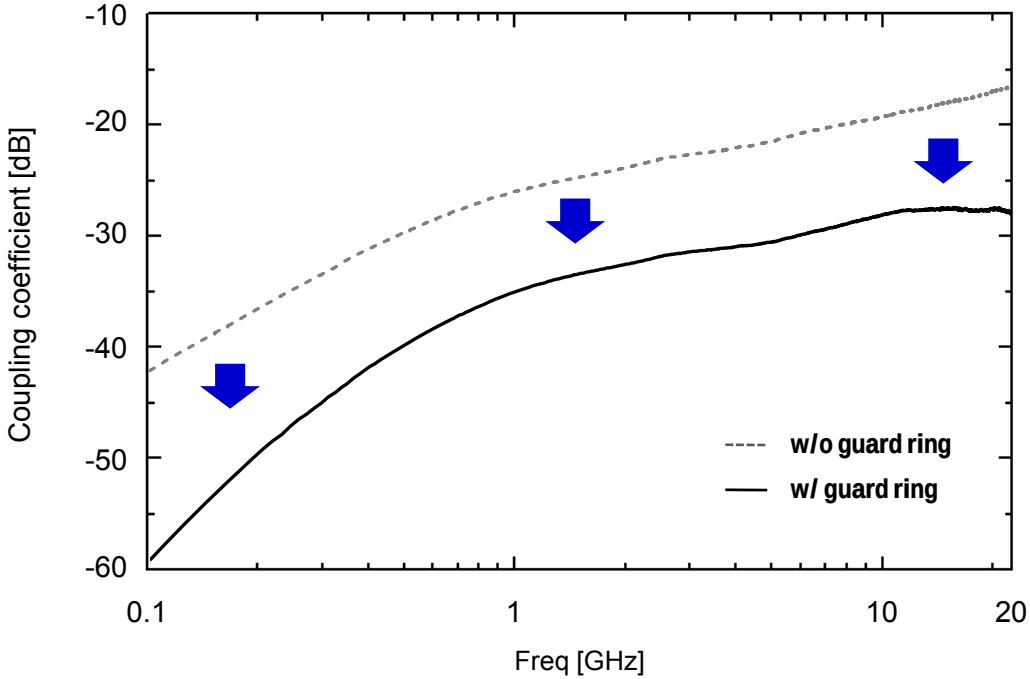
Shielding Effect Measurement– (2) Guard Ring



< Top view>

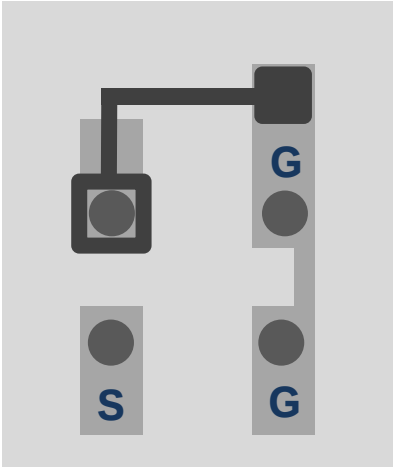


< Equivalent circuit model of coupled TSV>

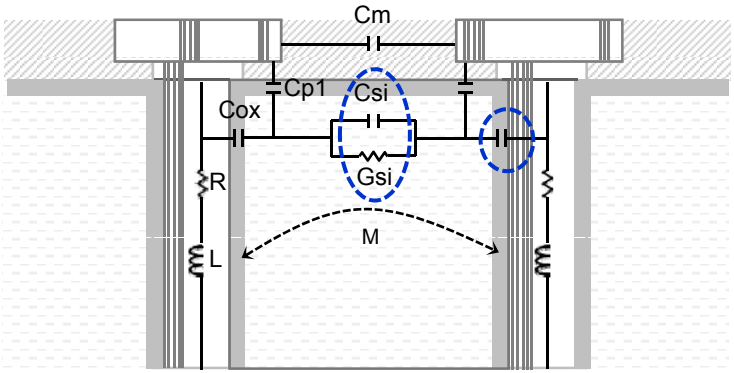


- **Guard ring has good shielding effect in every frequency range because guard ring structure can partly block substrate coupling between TSVs**
- Main factor of coupling between TSVs is silicon substrate

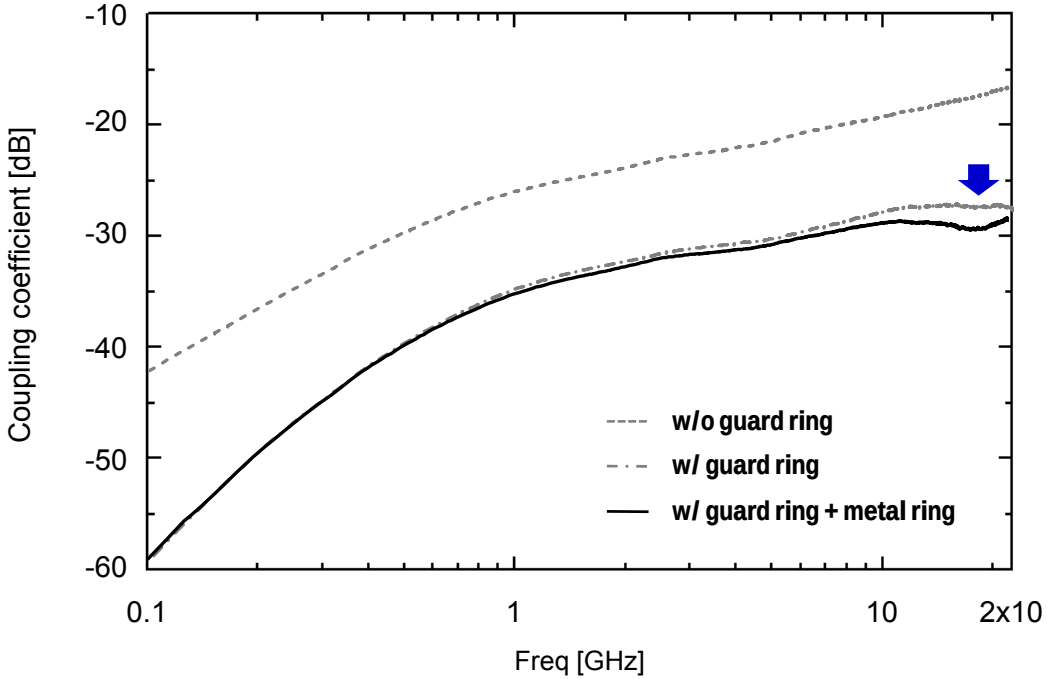
Shielding Effect Measurement– (3) Guard Ring + Metal Ring



< Top view>

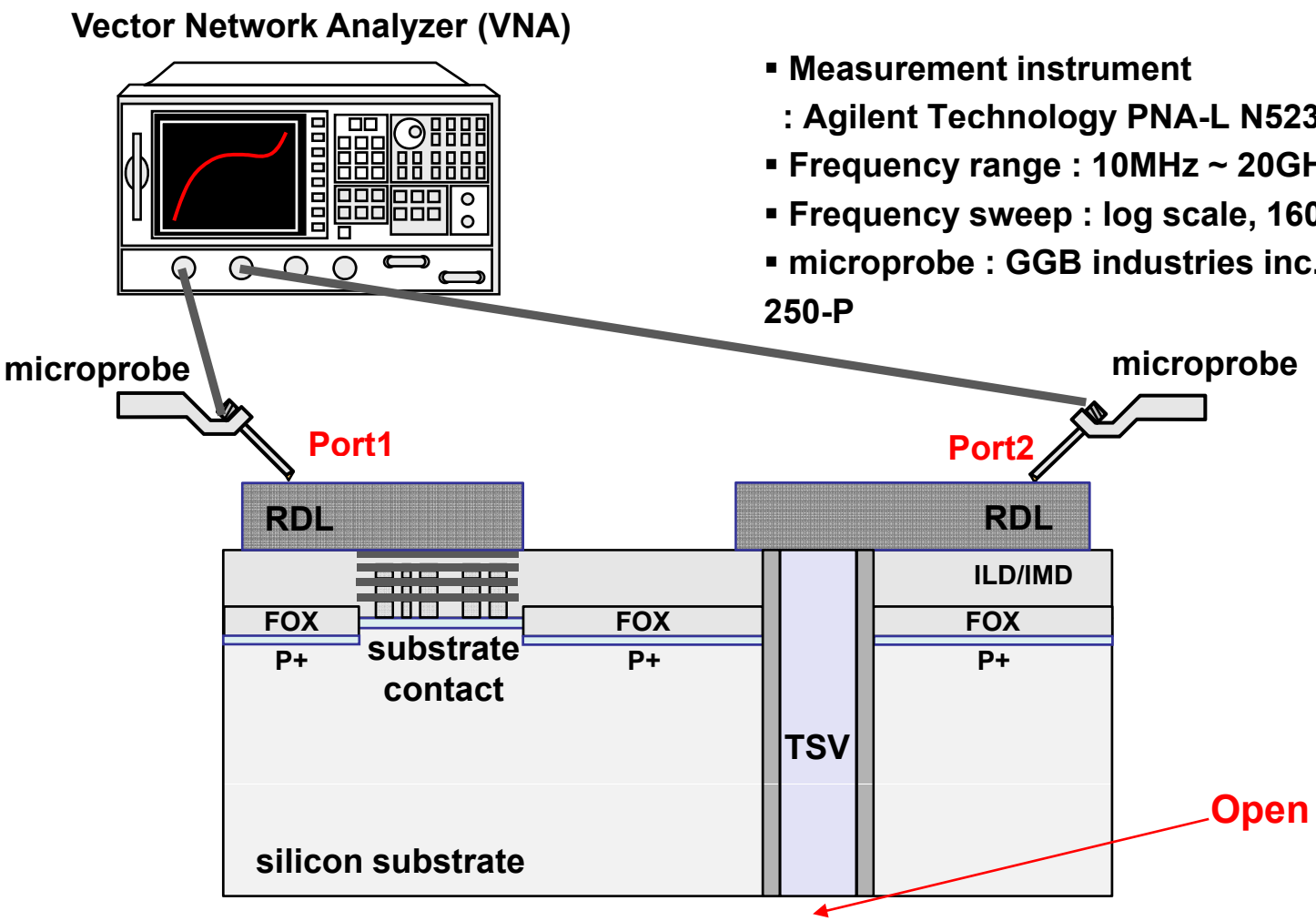


< Equivalent circuit model of coupled TSV>



- **Metal ring structure with guard ring can further decrease coupling between TSVs**

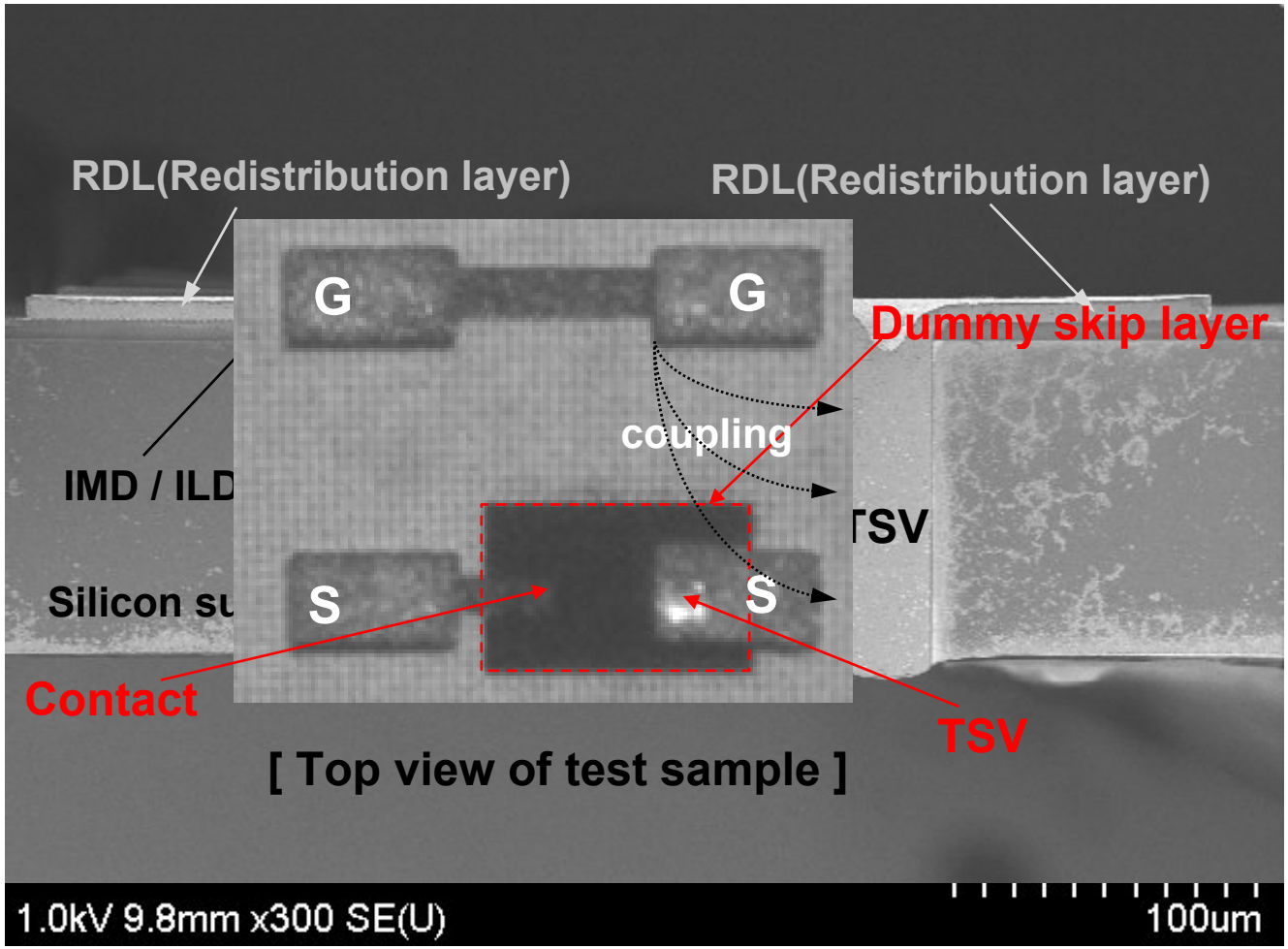
Measurement Environments for Model Verification



- Measurement instrument
  : Agilent Technology PNA-L N5230A
- Frequency range : 10MHz ~ 20GHz
- Frequency sweep : log scale, 1601 point
- microprobe : GGB industries inc. 40A-GS-250-P

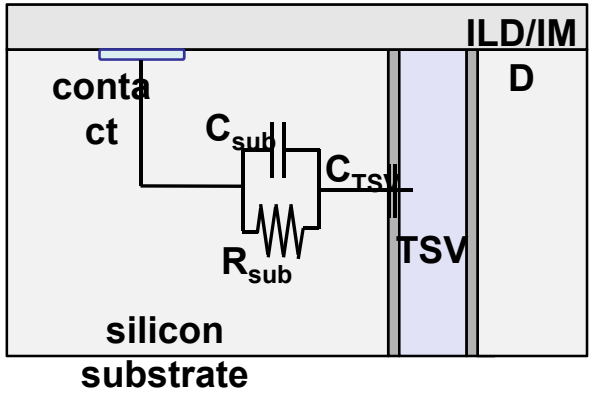
[Cross sectional view of test sample]

Designed Test Sample Images



[Cross sectional view of test sample]

Analysis of Noise Coupling based on the 3D TLM Model

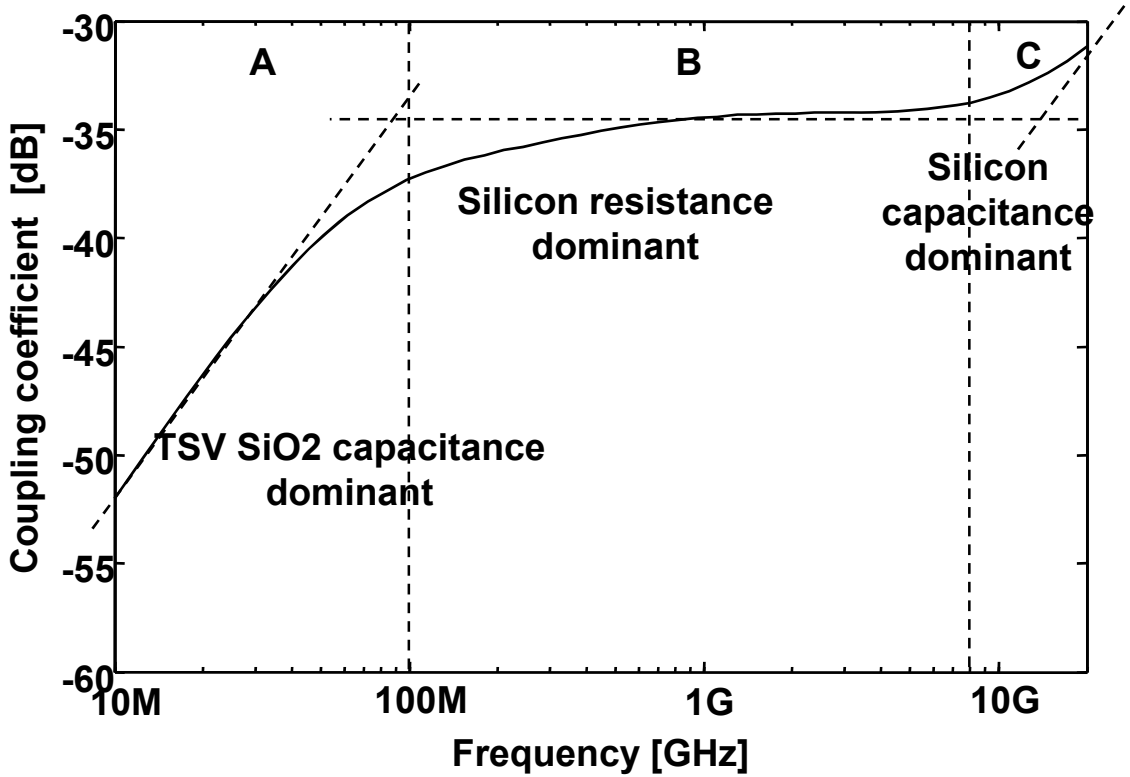


Distance between contact and TSV : 100 μm

Substrate height : 100 μm

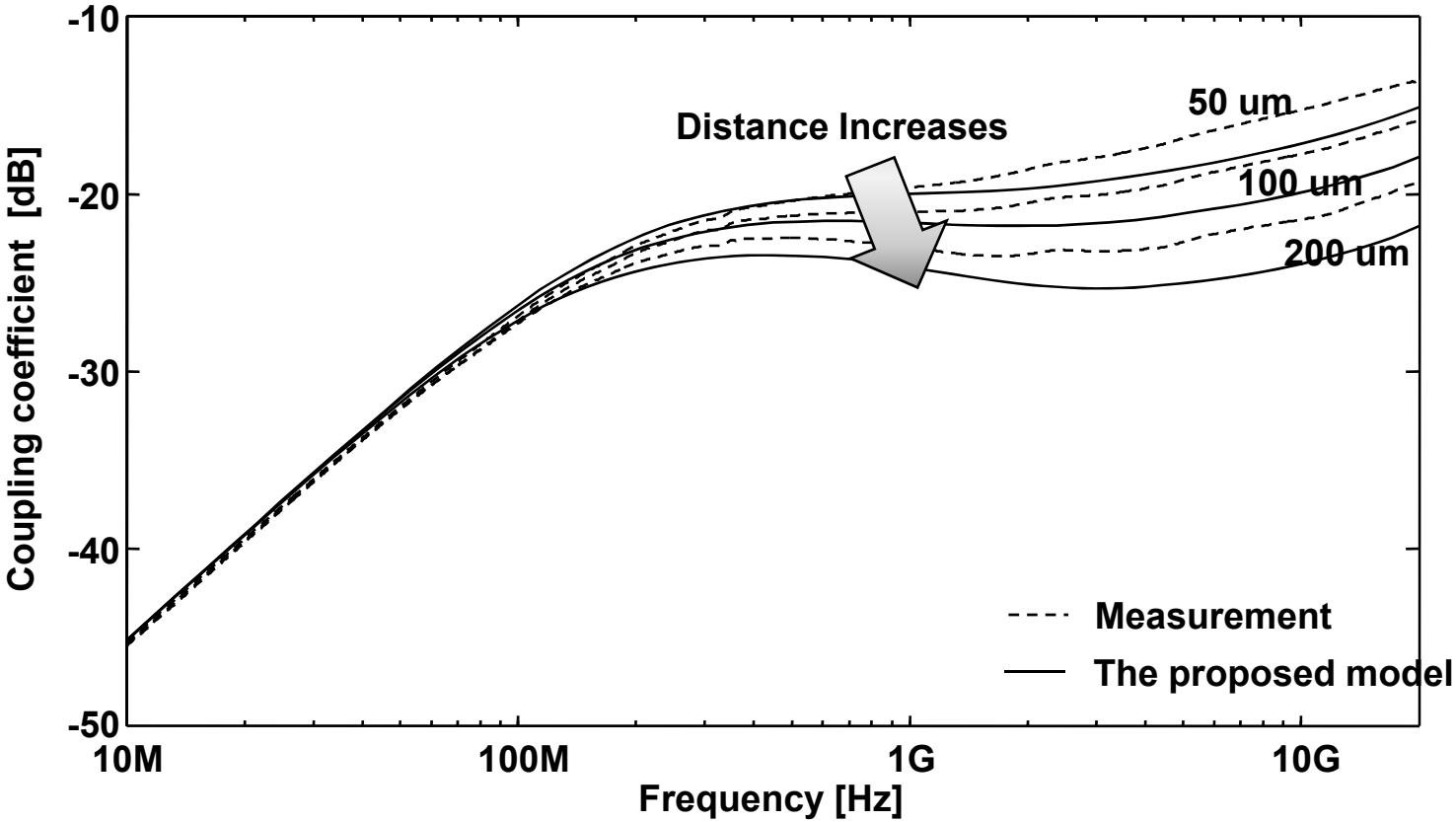
TSV diameter : 30 μm

TSV SiO_2 thickness : 0.5 μm



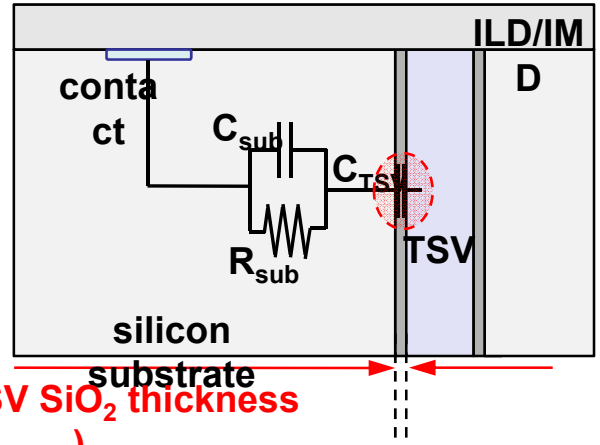
- Coupling can be divided into 3-regions
- In region A, B, and C TSV SiO_2 capacitance , silicon resistance, silicon capacitance is the dominant factor to the coupling

Substrate contact to TSV Coupling 3D TLM Model Verification by Measurement – with Distance Variation



- Proposed model's coupling coefficient estimation is less than measurement over 1GHz
- But model follows same tendency as the distance increases

Analysis of Noise Coupling based on the 3D TLM Model – with TSV SiO_2 Thickness Variation



TSV SiO_2 thickness (t_{ox_TSV})

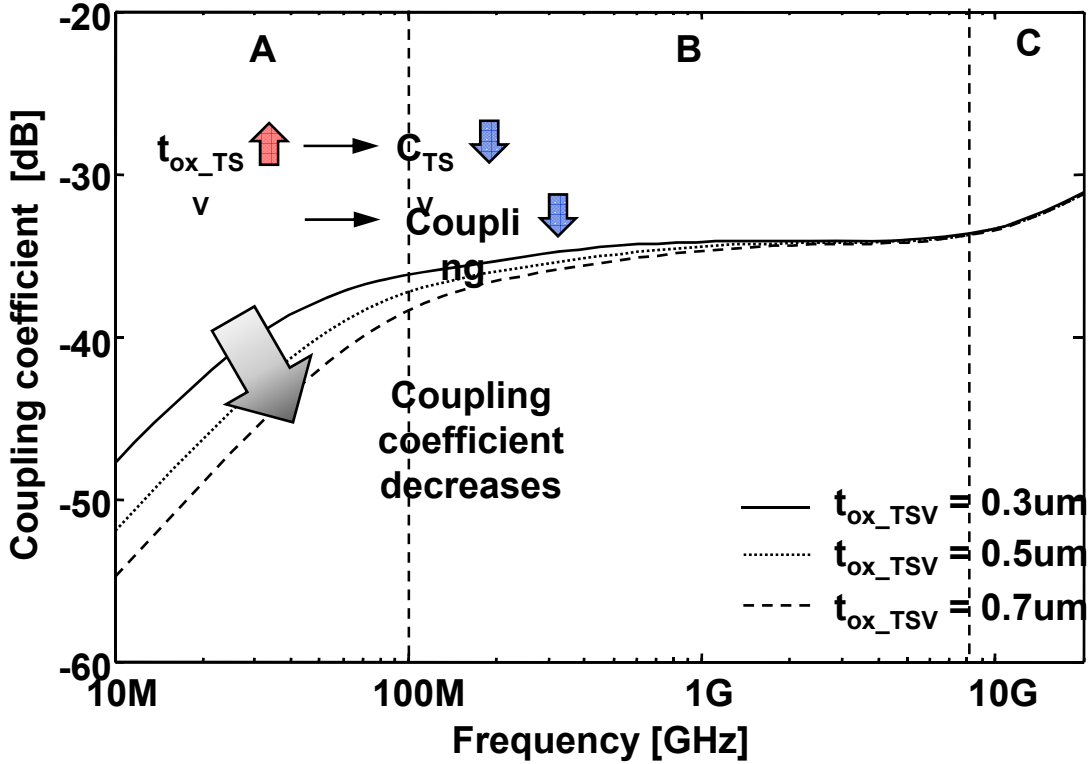
Distance between contact and TSV : 100 μm

Substrate height : 100 μm

TSV diameter : 30 μm

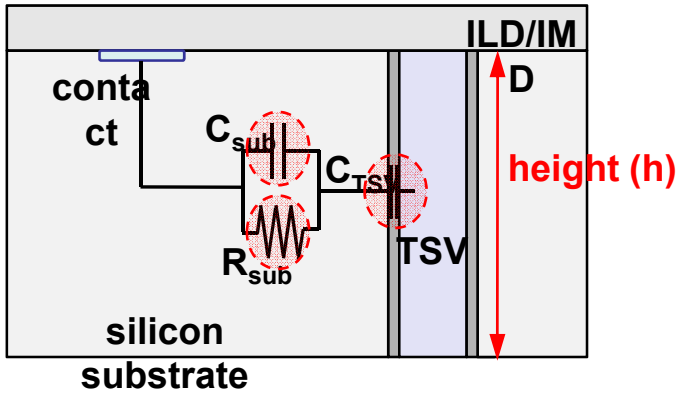
TSV SiO_2 thickness : 0.3, 0.5, 0.7 μm

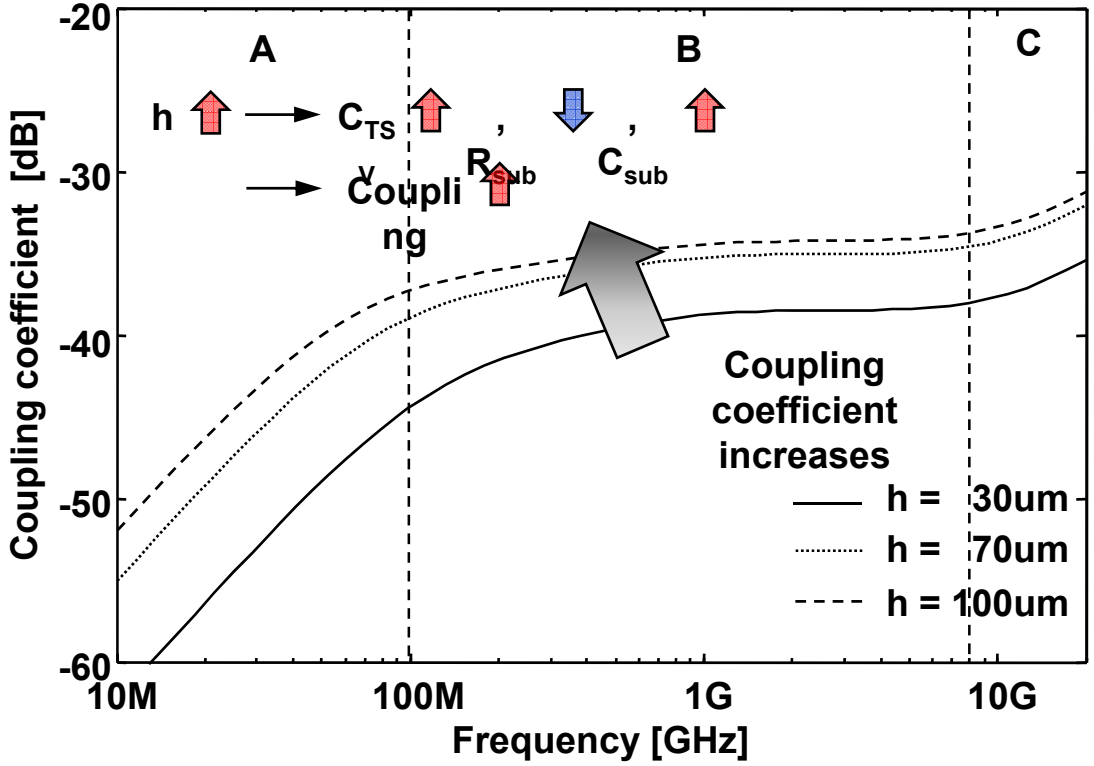
Substrate conductivity : 10S/m



- TSV SiO_2 thickness determine the coupling coefficient in the region A
- If we increases TSV SiO_2 thickness, coupling coefficient decreases in the region A

Analysis of Noise Coupling based on the 3D TLM Model – with Silicon substrate Height Variation (1)





Distance between contact and TSV : 100 μm

Substrate height : 30, 70, 100 μm

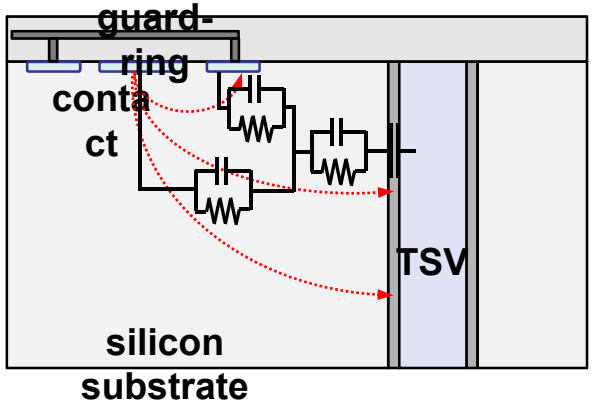
TSV diameter : 30 μm

TSV SiO_2 thickness : 0.3 μm

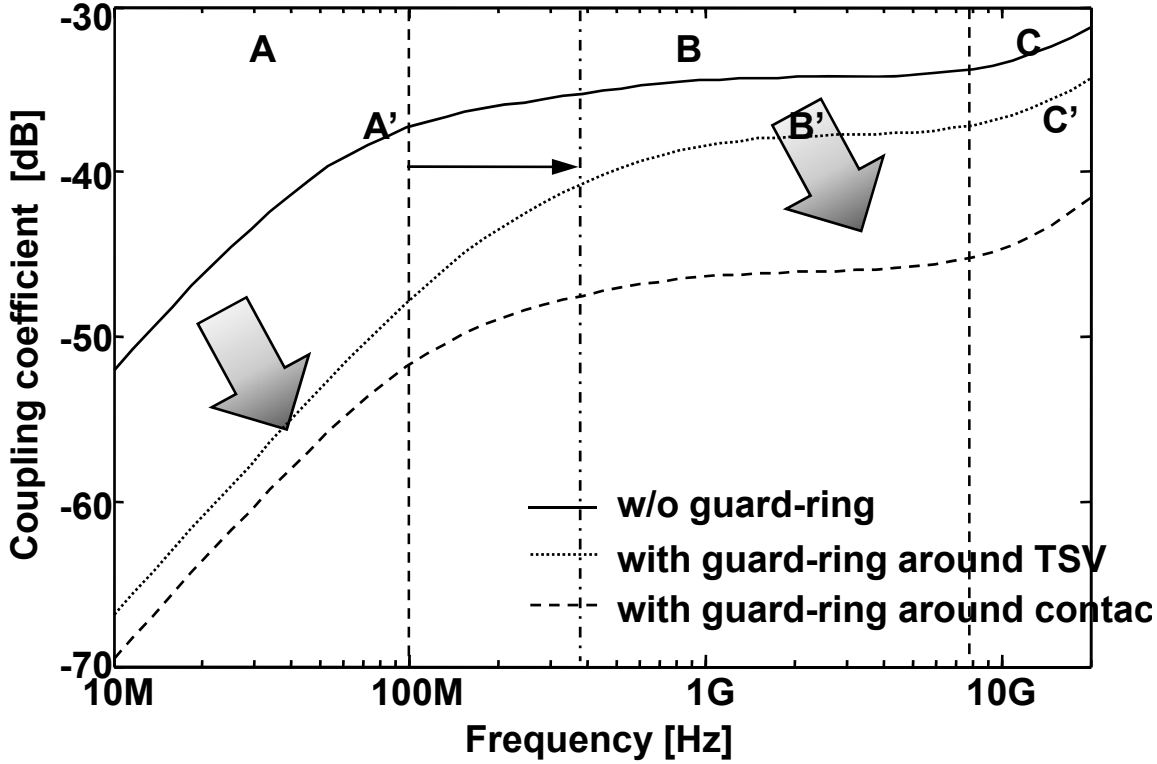
Substrate conductivity : 10S/m

- If silicon substrate height decreases, all component value is changed
- At the whole frequency, the coupling coefficient increases as silicon substrate height increases

Analysis of Guard-ring based on the 3D TLM Model – with Guard-ring Location Variation

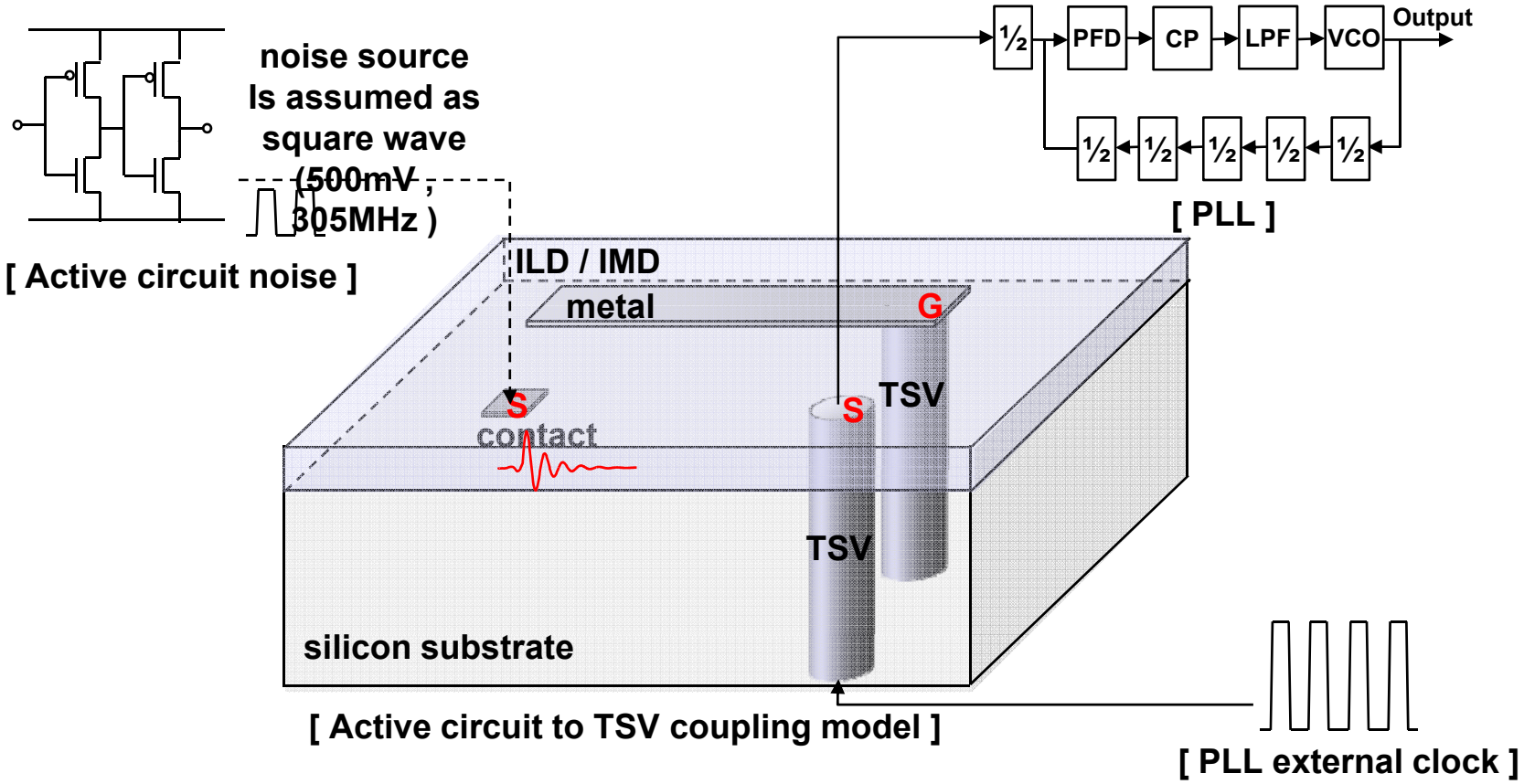


Distance between contact and TSV : 100 μm
Substrate height : 100 μm
TSV diameter : 30 μm
TSV SiO_2 thickness : 0.5 μm
Guard-ring distance from contact : 10 μm
Guard-ring width : 10 μm



- Guard-ring around contact shows more isolation effect compared to guard-ring around TSV
- Guard-ring around contact does not have frequency dependent isolation effect

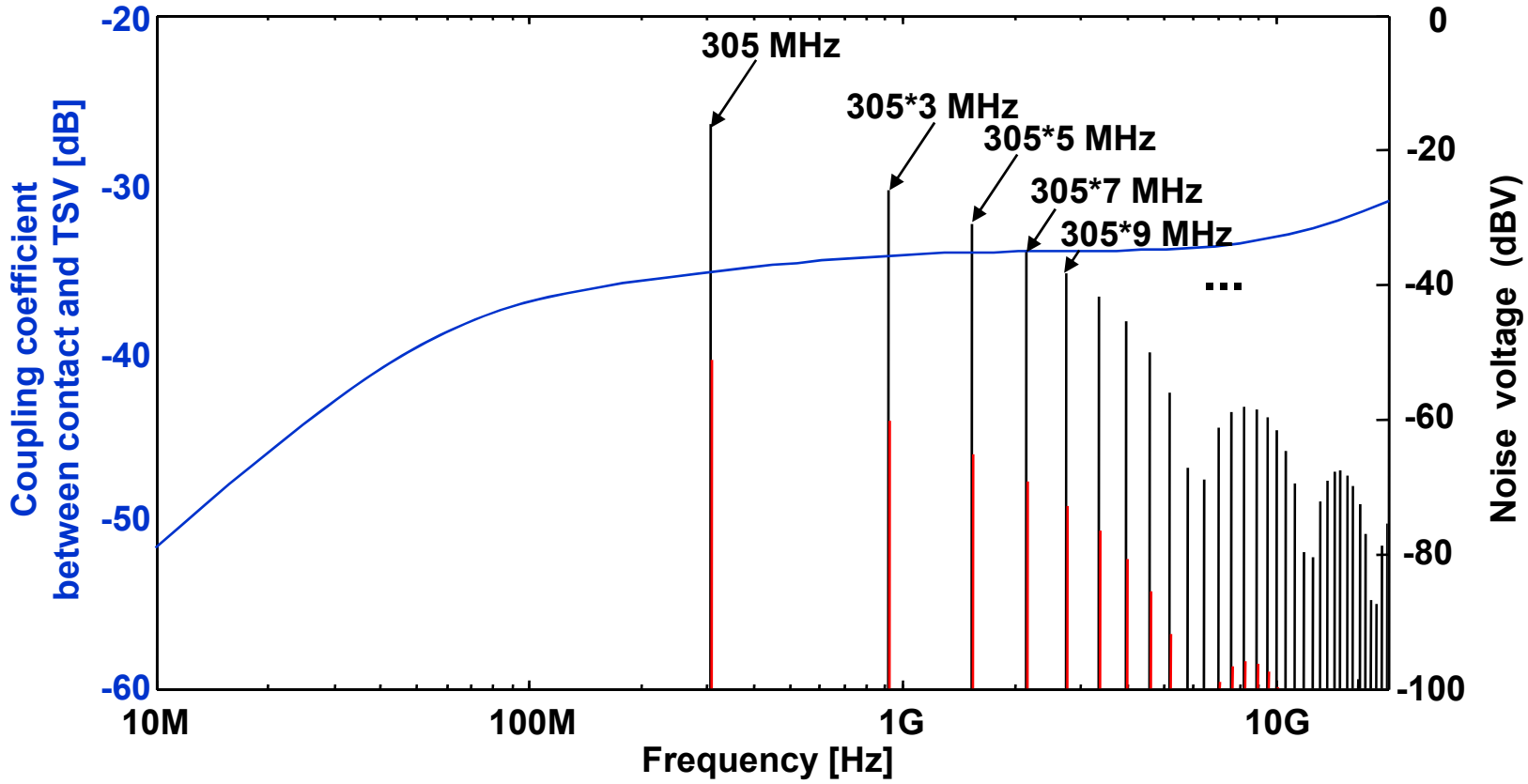
PLL Coupling Simulation Environment



- Contact to TSV coupling model was proposed and verified in the previous chapter

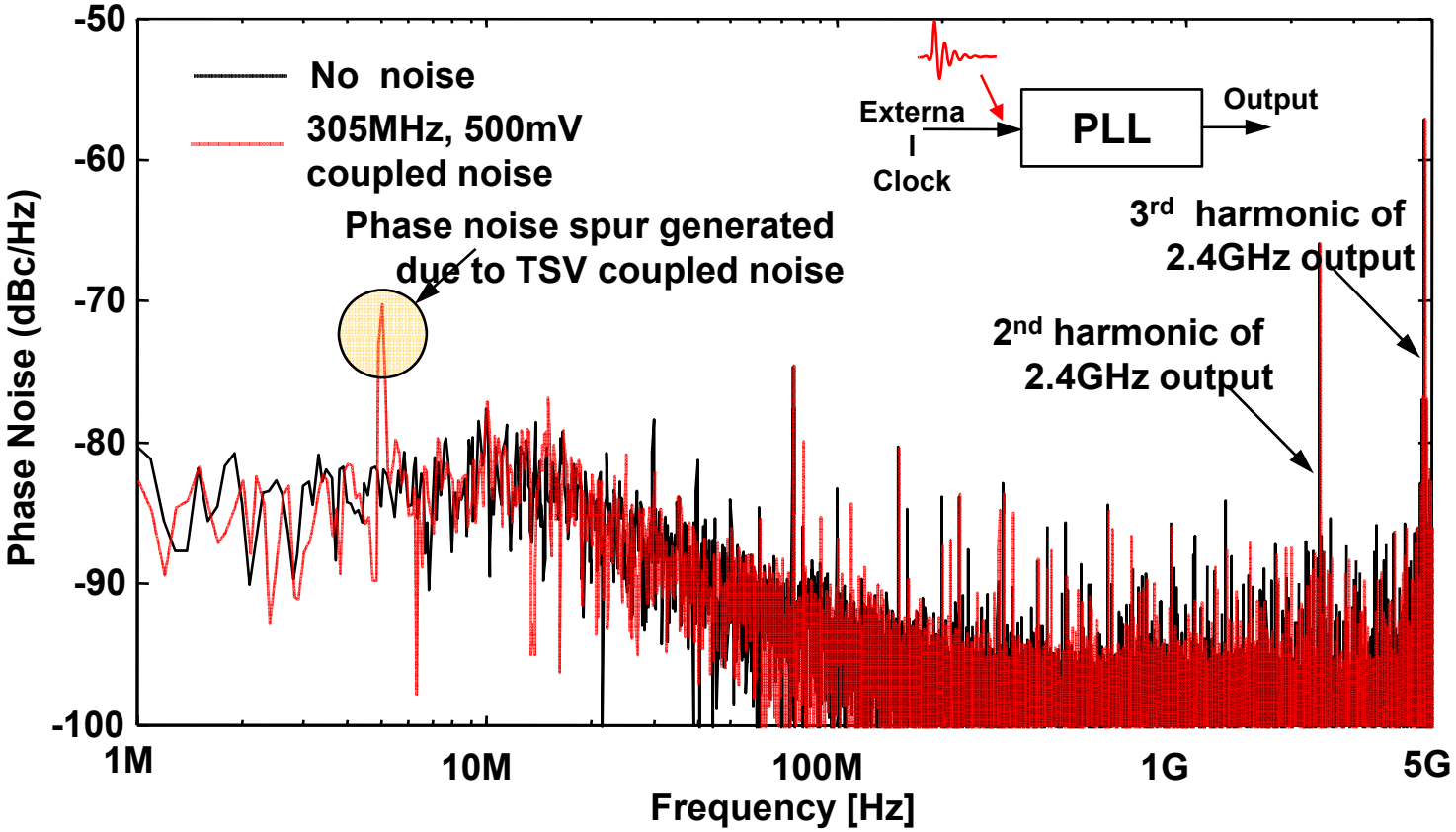
- HSPICE simulation was performed using the contact to TSV coupling model and PLL schematic

Substrate Noise Coupling to TSV



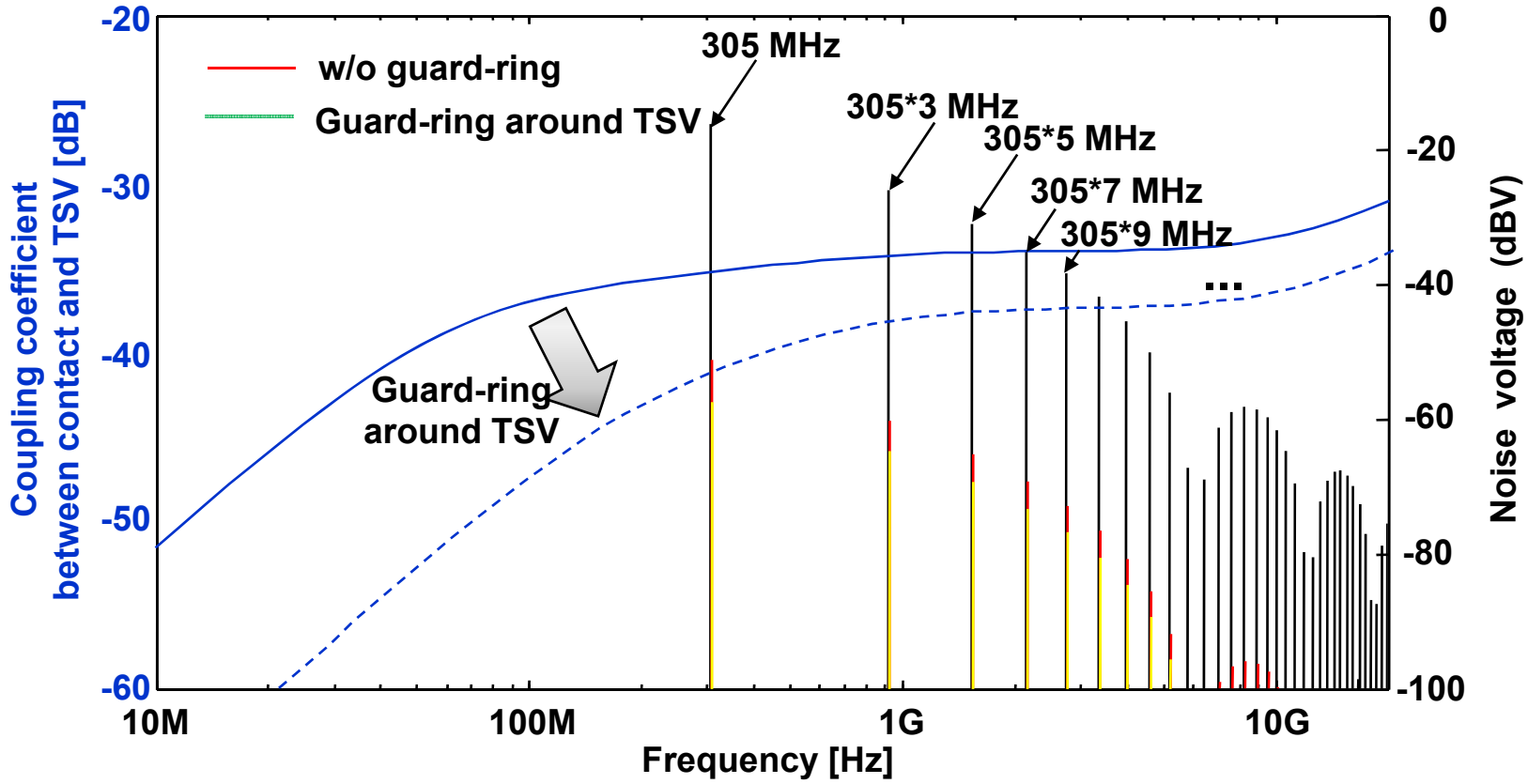
- 305MHz square wave noise is coupled to TSV by the coupling coefficient
- Up to 9th harmonic frequency, coupling coefficient is almost constant

PLL Phase Noise Degradation due to Active Circuit to TSV Coupling



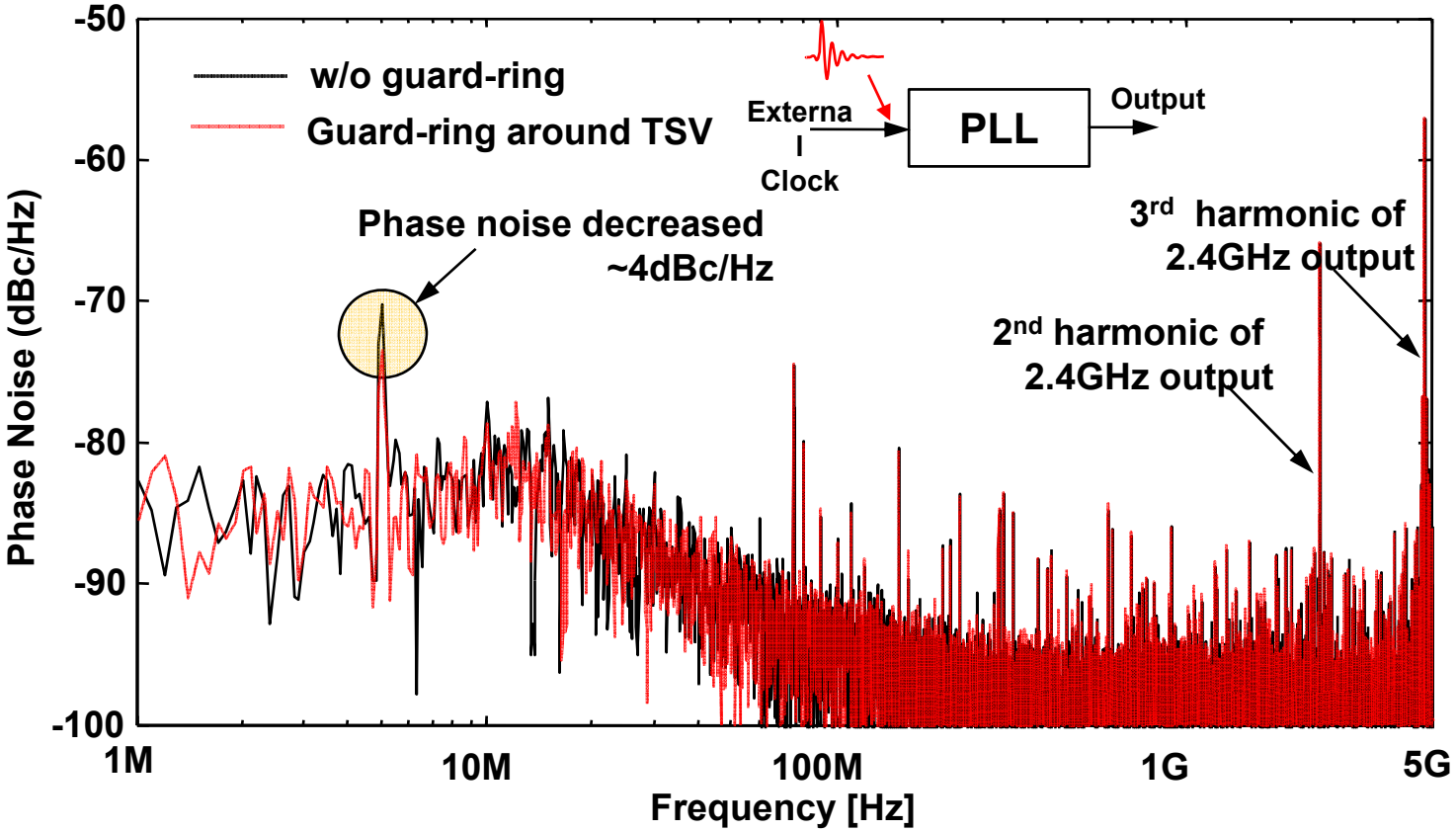
- PLL phase noise shows spurs at 5MHz due to coupled 305MHz noise
- PLL phase noise spur at 75MHz, 2.4GHz, 4.8GHz is due to circuit design

Substrate Noise Coupling to TSV



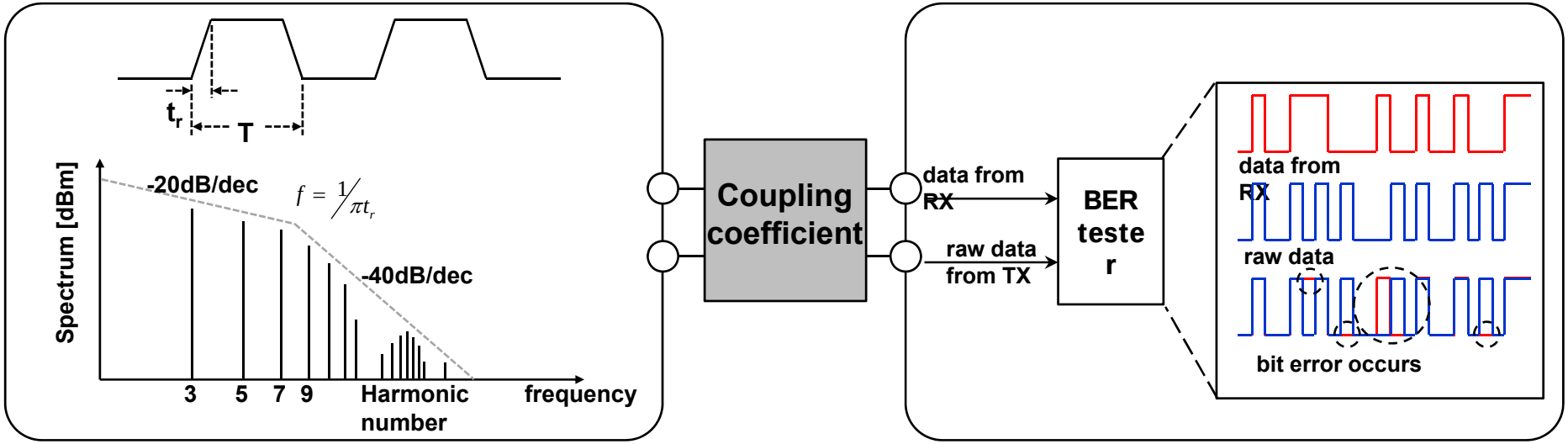
- Guard-ring around TSV decreased coupling coefficient
- PLL coupled noise also decreased by the guard-ring around TSV

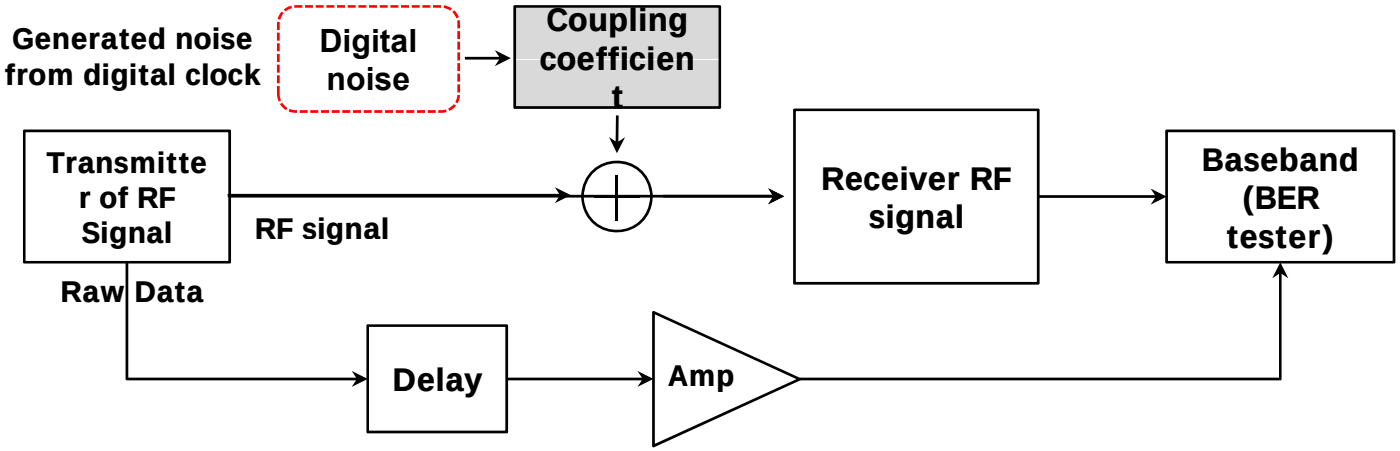
PLL Phase Noise Degradation due to Active Circuit to TSV Coupling



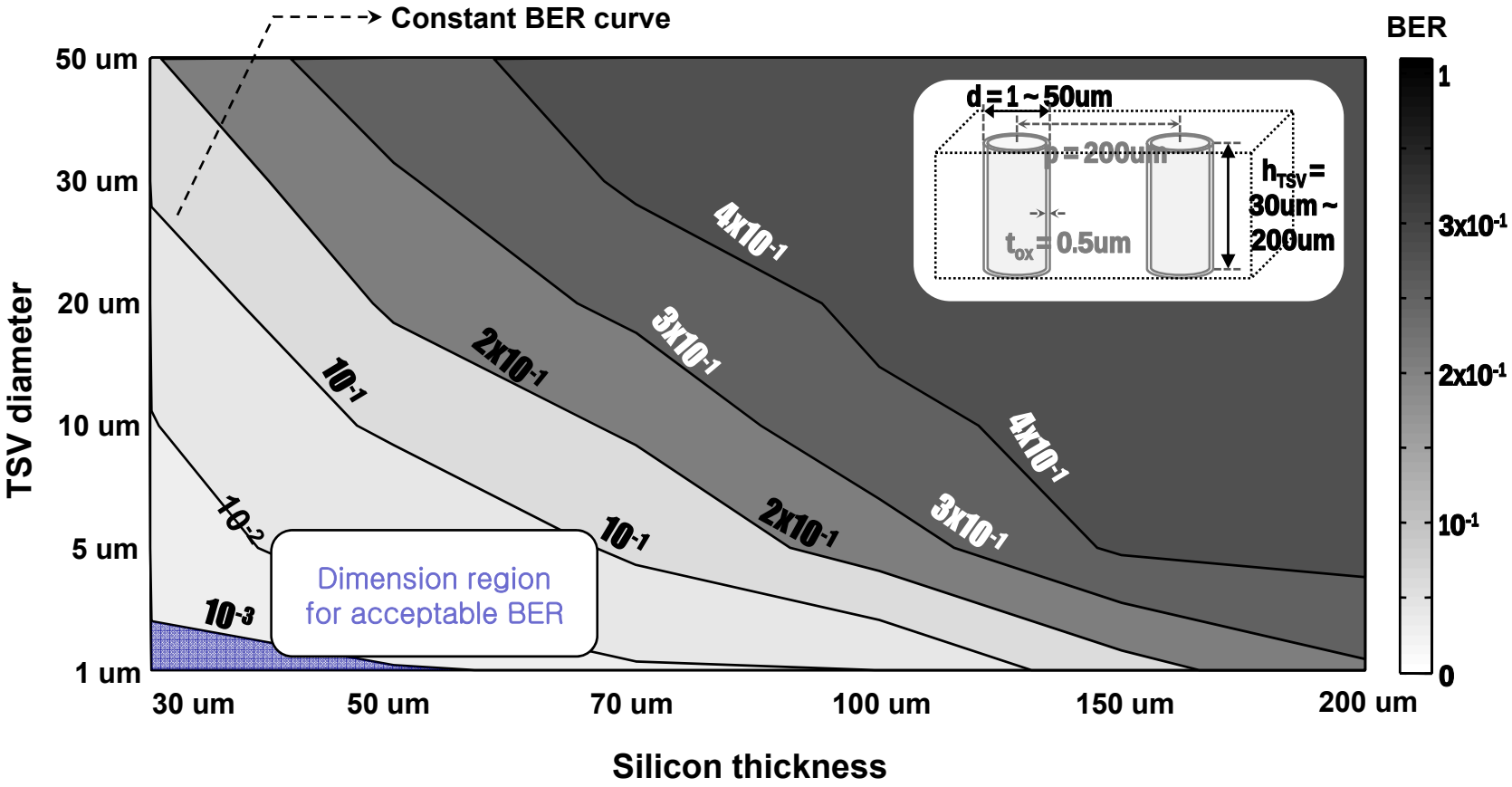
- PLL phase noise spur at 5 MHz decreased by the guard-ring
- Guard-ring around TSV can improve coupling degraded circuit performance

BER Calculation in Mixed-Signal System Model



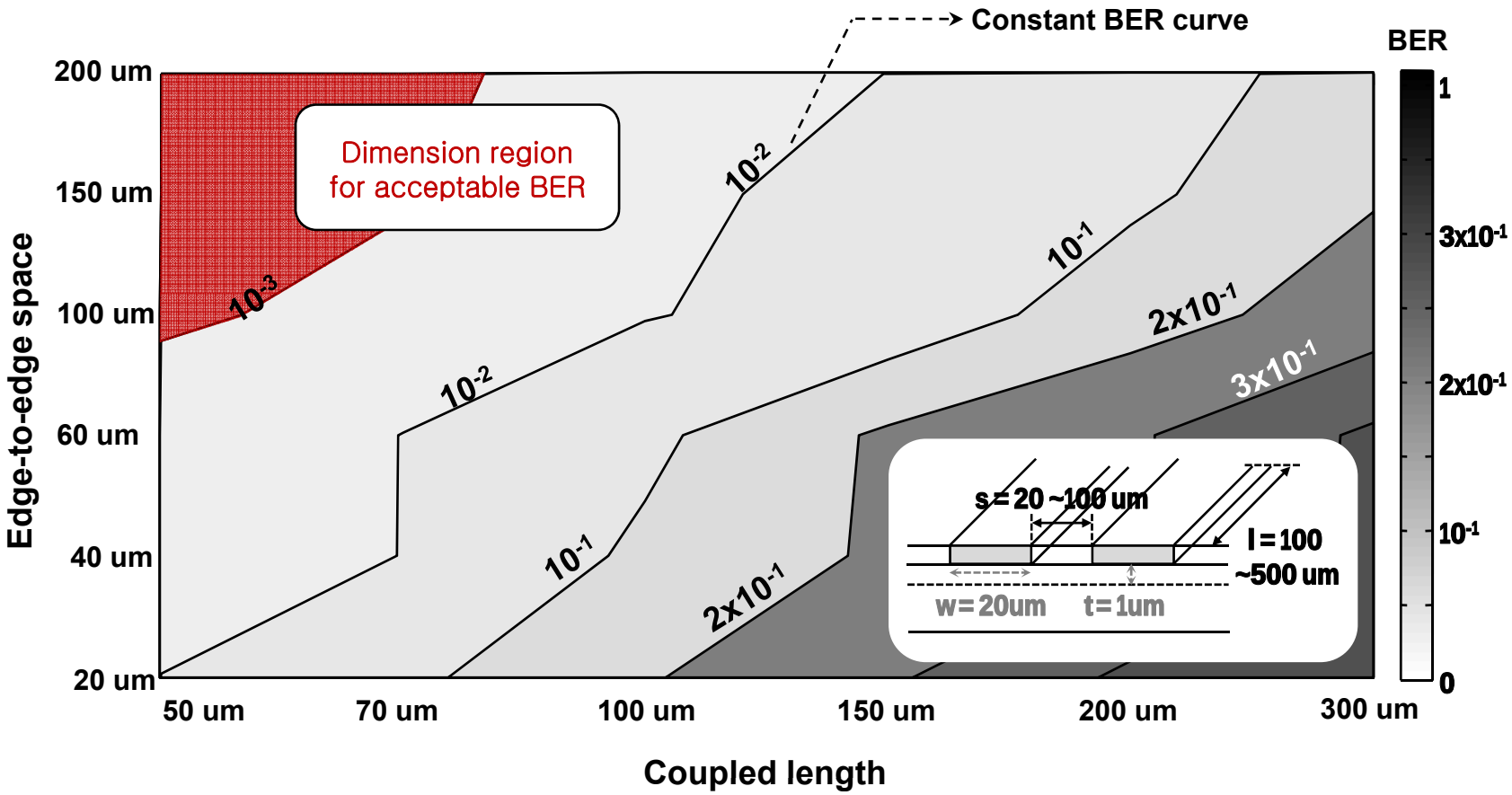


Dimension Region with Coupled TSV Parameters



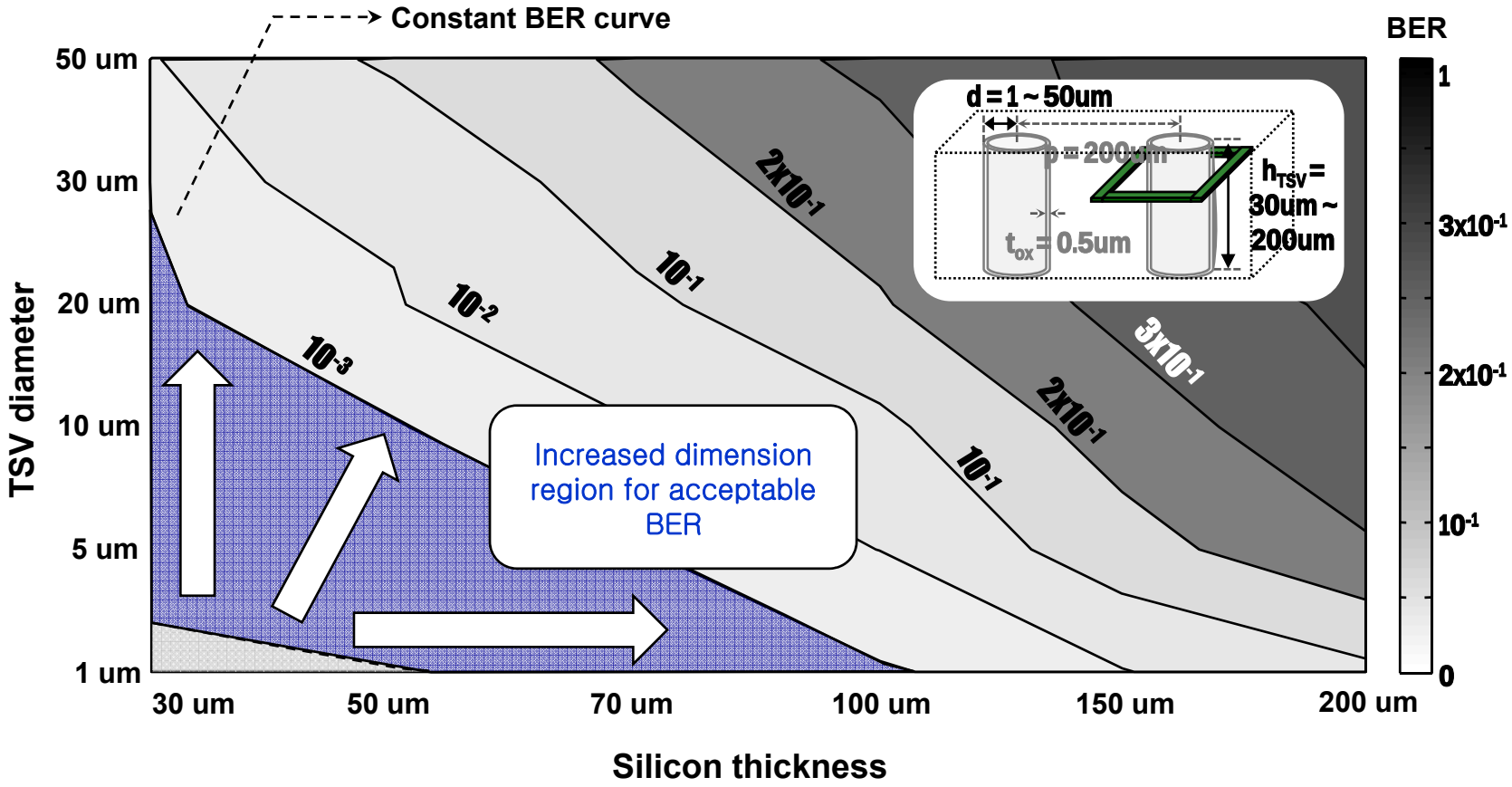
- **In certain digital application, dimension region of TSV design parameters for acceptable BER can be obtained from the modeling of coupled TSVs**

Dimension Region with Coupled RDL Parameters



- In certain digital application, dimension region of RDL interconnects design parameters for acceptable BER can be obtained from the modeling of coupled RDL interconnects

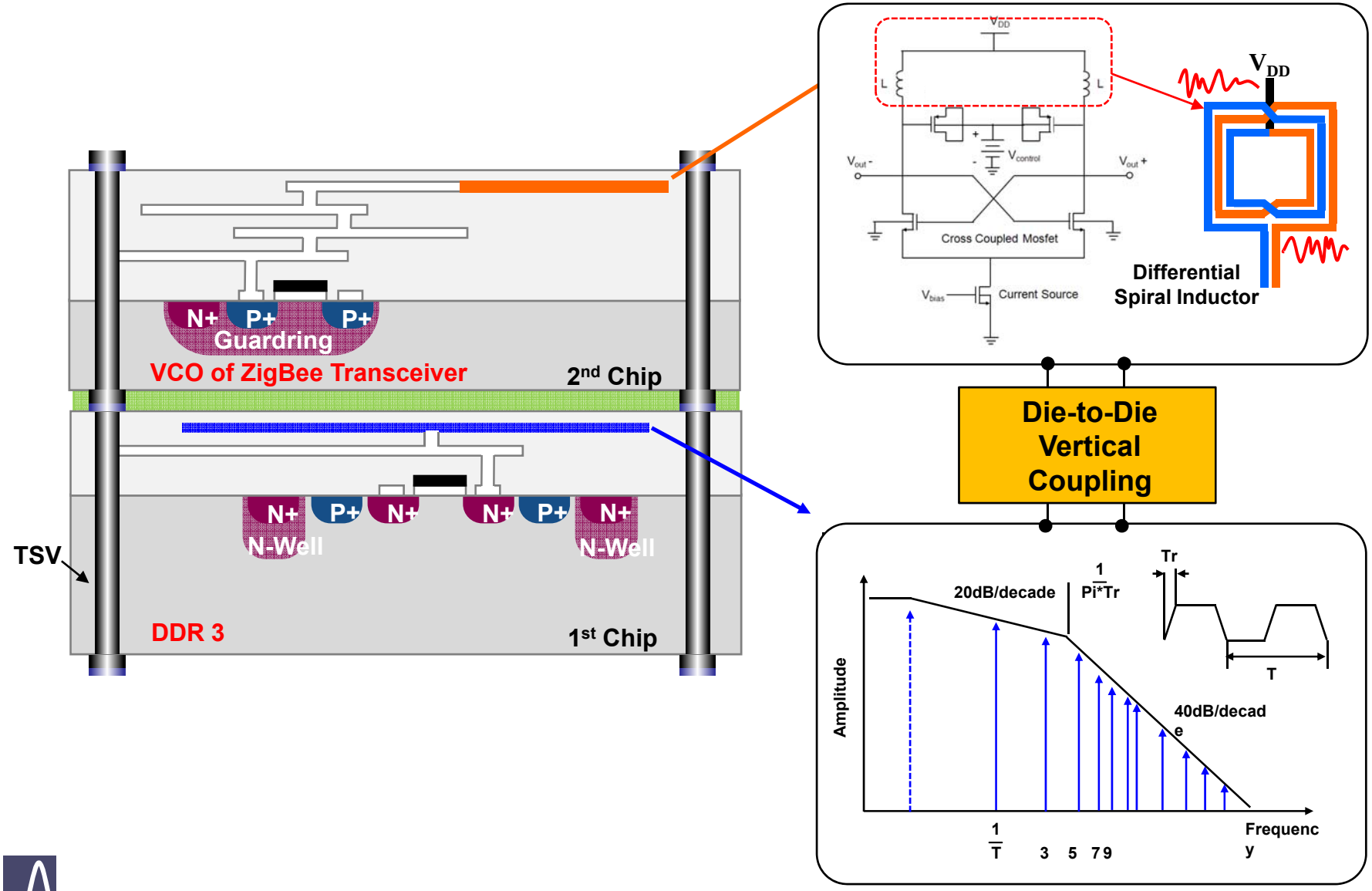
Dimension Region with Coupled TSV Parameters with Guard Ring



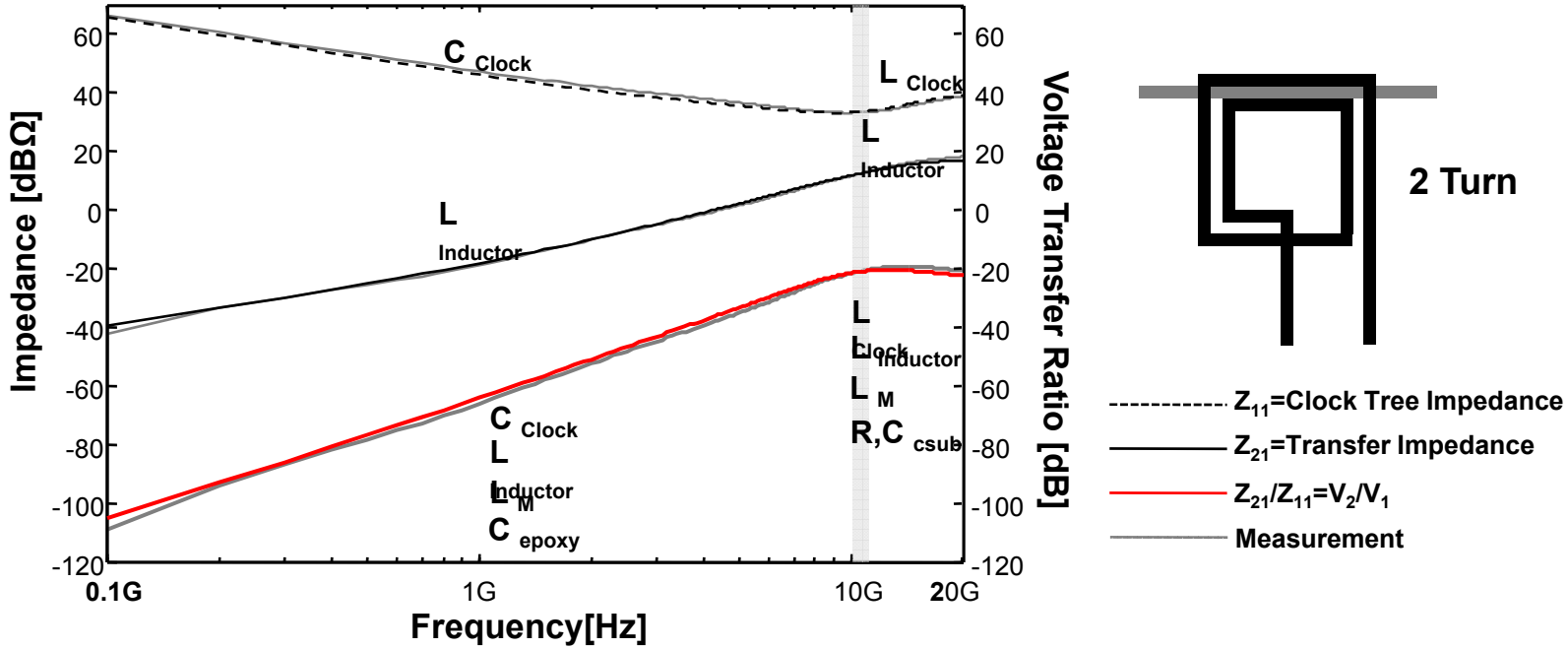
- By applying guard ring structure, dimension region for acceptable BER is significantly increased

→ Target BER can be satisfied within realizable dimensions

Vertical Coupling of DDR3 to ZigBee Transceiver

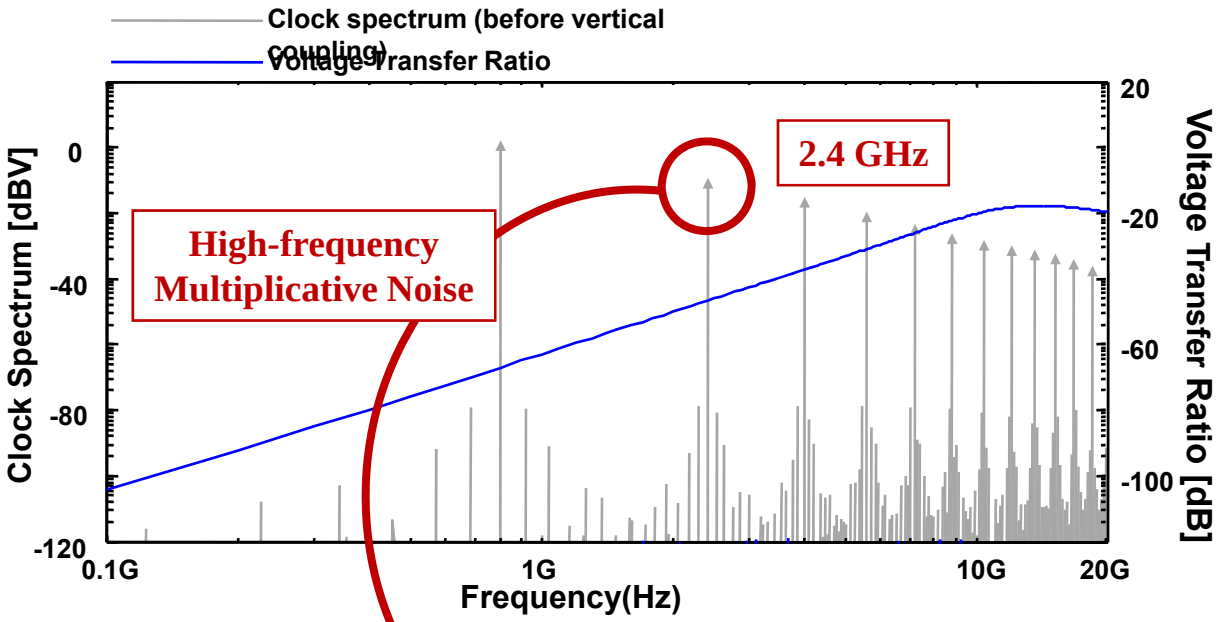


Experimental Verification of Proposed Model (Line Type Clock Tree to Two Turn Spiral Inductor)



- Before clock tree resonance, voltage transfer ratio is determined by C_{clock} and $L_{inductor}$.
- After clock tree resonance, voltage transfer ratio is determined by L_{clock} and $L_{inductor}$.

Investigation of Vertical Coupling Effect on VCO Spur

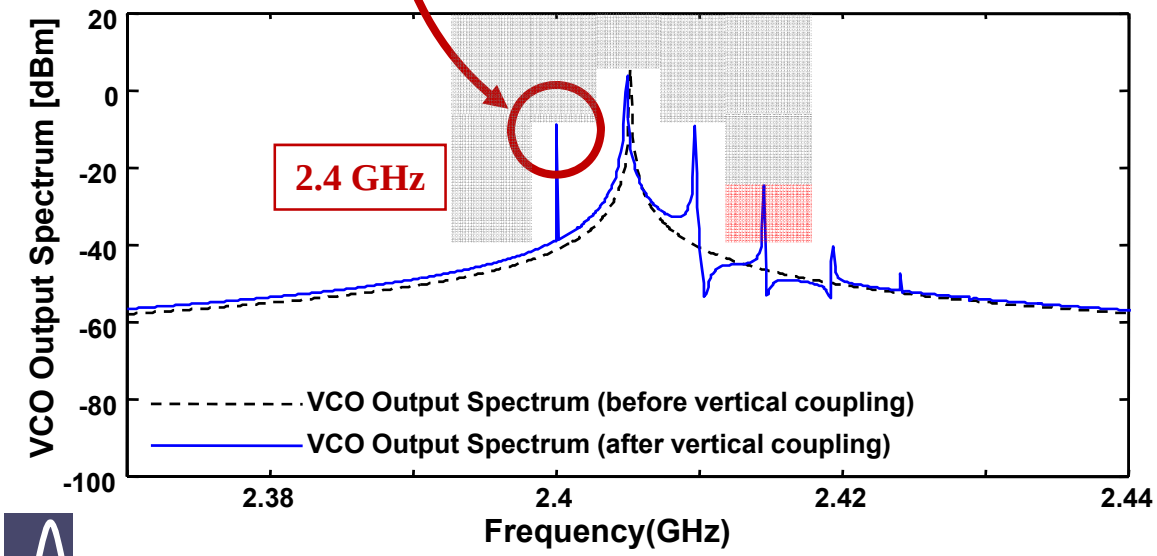


$$\frac{1}{A} = \frac{Z_{21}}{Z_{11}} = \frac{V_2/I_1}{V_1/I_1} = \frac{V_2}{V_1}$$

$$20\log(V_1 * \frac{1}{A})dB = 20\log(V_2)dB$$

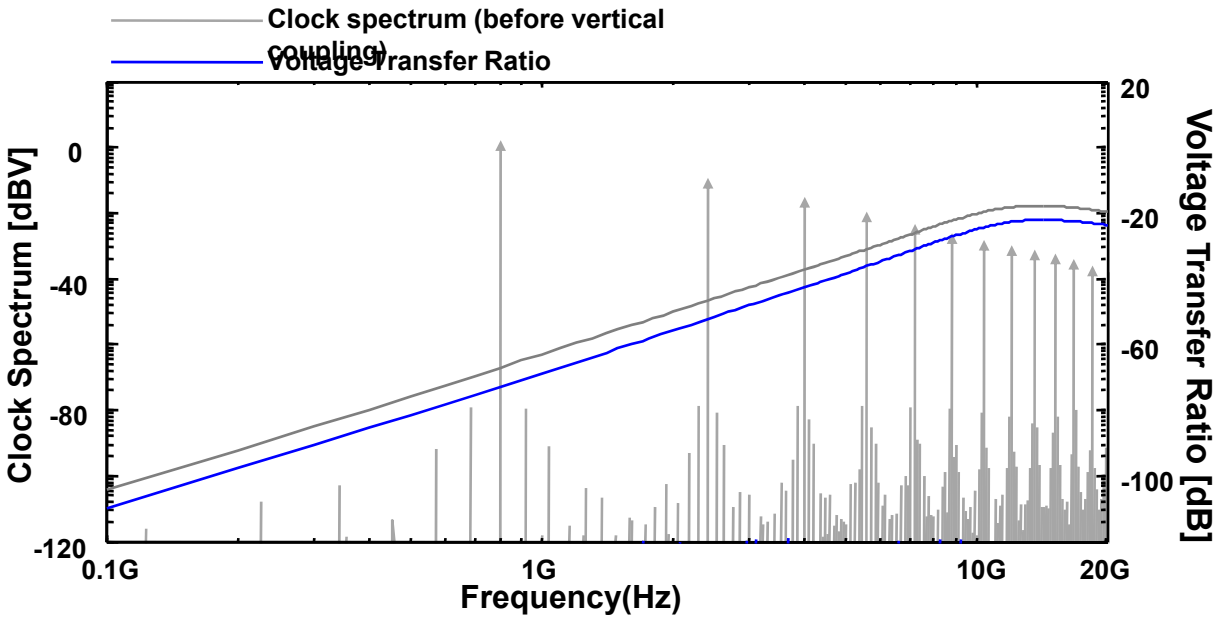
$$20\log(V_1)dB + 20\log(\frac{1}{A})dB$$

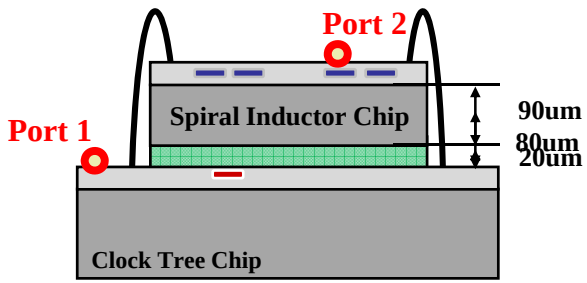
$$= 20\log(V_2)dB$$

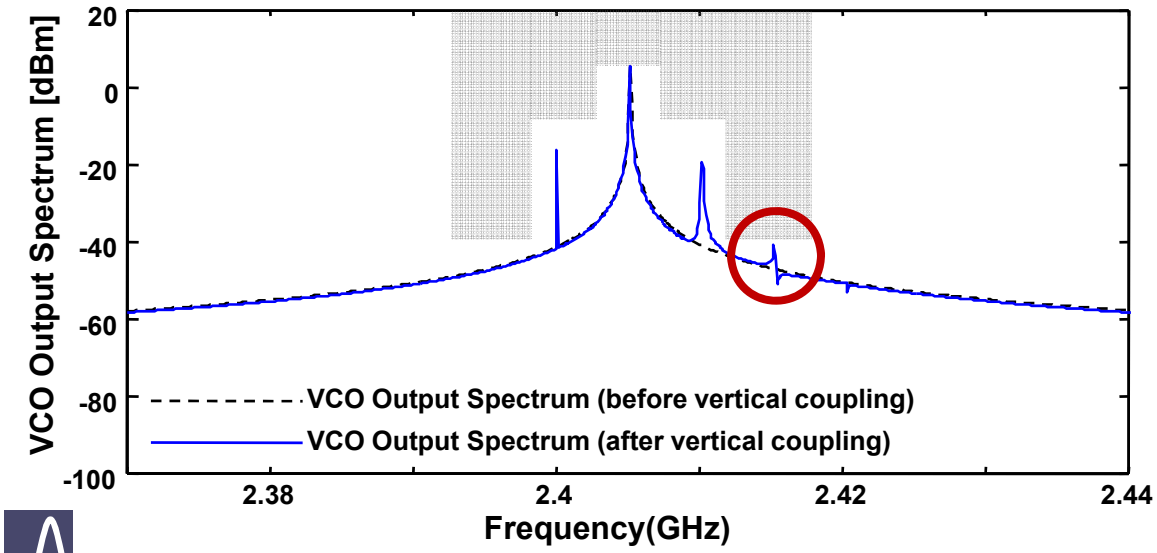


- **Main mechanism of spur generation is high-frequency multiplicative noise**
- **To reduce the spur at 10MHz offset from center frequency, design guide has to be proposed.**

Investigation of Design Guide for Spur Reduction (Epoxy Thickness)







- Spurs at 5MHz and 10MHz offset from center frequency satisfy the spur spec of ZigBee system.
- Increasing epoxy thickness is highly effective for spur reduction.

Summary

-TSV is the most critical interconnection structure in 3D IC.

- TSV can cause significant channel loss for high-speed signaling.

- Equalizer or specific I/O schemes are needed to support low power and high-speed data transmissions.

- Crosstalk and coupling between TSV and active circuit need to be considered when designing the TSV arrangement configurations.

- Shielding structures are needed to reduce the TSV crosstalks and noise couplings.