Introduction to Digital Logic
Missouri S&T University CPE 2210
Flip-Flops

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Flip-Flops

Outline

• Introduction
• Flip-flops and types
• Summary
Digital Logic
Circuit Types

- What are the type of digital circuits?
Digital Logic
Circuit Types

• What are the type of digital circuits?
• Combinatorial
  – output solely depends on present values of input(s)
    • no memory
  – basic blocks of circuits
  – e.g.: lamp with light sensor
• Sequential
  – output depends on present and past values of input(s)
    • output depends on present state
  – e.g.: calculator
Sequential Logic Circuits

Examples

• *What are examples of sequential circuit elements?*
Sequential Logic Circuits

Examples

- Examples of sequential logic elements:
  - Latches
  - Flip-flops
  - Registers
  - Controllers
  - Counters
Basic SR Latch
Using NOR Gates

- We can change state of simple memory using latch
- NOR gates are connected cross-coupled style

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>( t (\overline{Q}) )</th>
<th>( Q )</th>
<th>Δno change</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1/0</td>
<td>0/1</td>
<td>no change</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
Level-Sensitive SR Latch Circuit and Symbol

- SR latch with enable input is a level-sensitive SR latch
- C is the enable input

<table>
<thead>
<tr>
<th>C</th>
<th>S</th>
<th>R</th>
<th>Q(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>x</td>
<td>no change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>no change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>x</td>
</tr>
</tbody>
</table>

Level-sensitive SR latch symbol
Level-Sensitive D Latch
Circuit and Symbol

- SR latch with enable input and inverter is a D latch
- C is the enable input

<table>
<thead>
<tr>
<th>C</th>
<th>D</th>
<th>Q(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>no change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Review Question

Overview

• Can we do latch functions using NAND gates?
  – instead of NOR gates
Review Question

Overview

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Review Question
Overview

[Diagram showing a flip-flop circuit with D (Data), Clk, S (Set), R (Reset), Q, and Q̅ (Complement of Q).]

- At time $t_1$, the Clk signal transitions, affecting the flip-flop.
- At time $t_2$, the D (Data) signal is applied.
- At time $t_3$, the Q signal changes state.
- At time $t_4$, the Q̅ signal changes state.

Time progression illustrating the behavior of the flip-flop with respect to Clk, D, Q, and Q̅ signals.
D Latch Problem

Delay

• When C is 1, how many latches will the signal travel?
D Latch Problem

Delay

- When C is 1, how many latches will the signal travel?
- Depends on clk signal:
  - Clk_A: signal may travel through multiple latches
  - Clk_B: signal may travel through fewer latches
D Latch Problem

Delay

Short clock

Q1 doesn't change

Long clock

2nd latch set

Q1/D2
S2
R2
Q2

Clk
D1
Q1/D2
S2
R2
Q2

Clk
D1
Q1/D2
S2
R2
Q2

Clk
D1
Q1/D2
S2
R2
Q2

Clk
D1
Q1/D2
S2
R2
Q2

Clk
D1
Q1/D2
S2
R2
Q2
D Latch Problem

Delay

- Issue: how to adjust clock cycle for right timing?
- Can we design bit storage that only stores a value on the rising edge of the clock signal?
D Latch Problem
Delay

- **Issue:** how to adjust clock cycle for right timing?
- **Can we design bit storage that only stores a value on the rising edge of the clock signal?**

![Rising edges](image)

- **Level-sensitive vs. edge-triggered:**
  - level-sensitive: sensitive to signal level
  - edge-triggered: sensitive to rise/fall of the signal
Edge-Triggered D Flip-Flop
Master-Servant Design

- Flip-flop: stores 1 bit on clock edge
- D flip-flop uses two D latches
- Master-servant is one design, there are others
Edge-Triggered D Flip-Flop Timing Diagram

- **Clk=0**
  - master enabled, loads D, appears at Qm, servant disabled
- **Clk=1**
  - master disabled, Qm stays same
  - servant latch enabled, loads Qm, appears at Qs
Edge-Triggered D Flip-Flop
Symbols

Symbol for rising-edge triggered D flip-flop

Symbol for falling-edge triggered D flip-flop

rising edges

falling edges
Edge-Triggered D Flip-Flop Timing Diagram

• Solves problem of not knowing through how many latches a signal travels when C=1

• How many flip-flops does signal travel in each cycle

Two latches inside each flip-flop

D1 Q1

D2 Q2

D3 Q3

D4 Q4

Clk

Clk_A

Clk_B
Edge-Triggered D Flip-Flop
Timing Diagram

- Solves problem of not knowing through how many latches a signal travels when C=1
- How many flip-flops does signal travel in each cycle?
- Signal travels exactly one flip-flop per cycle

![Timing Diagram](image_url)
D Latch vs. D Flip-Flop
Comparison

• Latch is level-sensitive, stores D when C=1
• Flip-flop is edge triggered, stores D when C 0→1

Latch follows D while Clk is 1
Flip-flop only loads D during Clk rising edge
Review Question

Overview

• Construct the timing diagram for the following
Construct the timing diagram for the following
SR Flip-Flop Overview

- Similar to SR latch
- However, instead of changing state with level change
- It changes state with edge rise/fall
SR Flip-Flop
Symbol and Characteristic Table

- SR flip-flop: Similar to SR latch, edge-triggered
T Flip-Flop
Overview

- T flip-flop: toggle flip-flop
- The output toggles on the rising edge of clock
- The circuit diagram:
T Flip-Flop
Symbol and Characteristic Table

- T flip-flop: toggle flip-flop
- The output toggles on the rising edge of clock

<table>
<thead>
<tr>
<th>T</th>
<th>Q(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Q(t)</td>
</tr>
<tr>
<td>1</td>
<td>Q'(t)</td>
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• T flip-flop: toggle flip-flop
• The output toggles on the rising edge of clock

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<td>Q(t)</td>
</tr>
<tr>
<td>1</td>
<td>Q'(t)</td>
</tr>
</tbody>
</table>

Clock

T

Q
• **T flip-flop**: toggle flip-flop
• The output toggles on the rising edge of clock

![Timing Diagram](image)

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<td>1</td>
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JK Flip-Flop

Overview

- JK flip-flop: combines features of SR and T flip-flops
- Instead of T only, we use J and K inputs
- \( D = JQ' + K'Q \)
- The circuit:

\[ D = JQ' + K'Q \]
JK Flip-Flop
Symbol and Characteristic Table

- JK flip-flop: toggle flip-flop

\[
\begin{array}{ccc}
\text{J} & \text{K} & Q(t+1) \\
0 & 0 & \text{no change } Q(t) \\
0 & 1 & 0 \\
1 & 0 & 1 \\
1 & 1 & \text{toggle } Q'(t) \\
\end{array}
\]
• It might be needed to have clear and preset button
• If clear is 0, Q is forced to be in 0
  – e.g. clear counter to be initial state to be 0
• If preset is 0, Q is forced to be in 1
  – e.g. insert specific value as initial value of a counter
Clock Signals
Overview

- Clock input is connected to clock signal
- It is from an oscillator signal
- Generates pulsing signal
- What is the period?
- What is the frequency?
- How many cycles are there?

<table>
<thead>
<tr>
<th>Time:</th>
<th>0 ns</th>
<th>10 ns</th>
<th>20 ns</th>
<th>30 ns</th>
<th>40 ns</th>
<th>50 ns</th>
<th>60 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clk</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Osc. → Clk
Clock Signals
Overview

- Clock input is connected to clock signal
- It is from an oscillator signal
- Generates pulsing signal
- What is the period? 20 ns
- What is the frequency? 1/20 ns = 50 MHz
- How many cycles are there? 3.5
Clock Signals
Overview

- Clock input is connected to clock signal
- It is from an oscillator signal
- Generates pulsing signal
- $T=1/f$
- **Synchronous circuit:**
  - storage elements change with clock
- **Asynchronous circuit:**
  - storage elements that does not use clock
Storing Multiple Bits
Registers

- Register: multiple flip-flops sharing common clock
- More about registers later
Flip-Flops

Summary

- Flip-flops store one bit
- Latches are level-sensitive
- **Flip-flops are edge-triggered**
- Signal travels one cycle per flip-flop
- D-flip-flops are most commonly used
- Flip-flop types: SR, JK, D, T
- Two types of flip-flops:
  - edge-triggered: active edge of the clock impacts the state
  - master-slave: with two gated latches
References and Further Reading

End of Foils