# Xilinx XC4005XL VGA Controller

## General Description

The VGA controller provides all functions necessary to drive a standard VGA compatible monitor from a microcontroller or microprocessor system. It exports a read-write framebuffer with room for 32x12 characters, although only 16x8 are displayed.

The VGA controller uses a flexible architecture that allows for easy expansion of framebuffer size or character set. It also displays the contents of the framebuffer during simulation so that correct interfacing can be verified.

Finally the device, including framebuffer, fits entirely in an XC4005XL part with about 10% room to spare for interfacing logic. This flexibility allows for easy interfacing to most microcontrollers.

## Applications

Embedded Process Control

Point of Sale Device

Hobbyist Projects

## Features

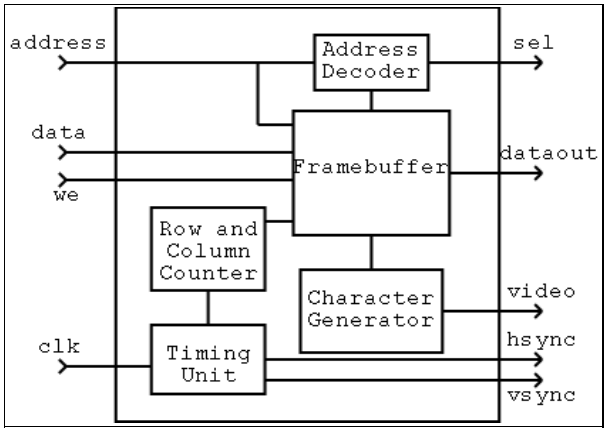
- **Flat 32x12 framebuffer**
- **Generates all required timing signals**
- **26 character font set**
- **Synthesizable into Xilinx XC4005XL part**
- **Read/Write framebuffer with address decoding logic**
- **Displays contents of framebuffer during simulation**

## Contact Information

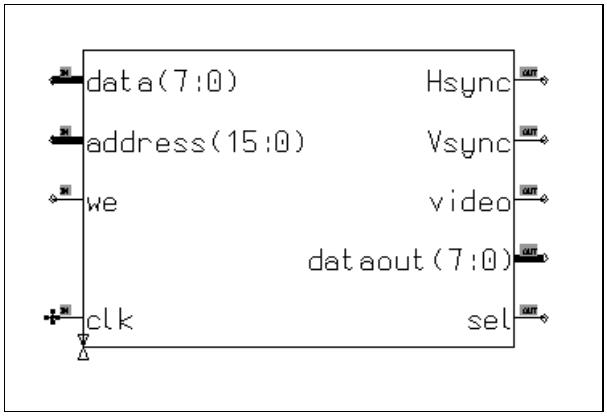
University of Missouri-Rolla
Department of Electrical and Computer Engr.
1870 Miner Circle
Rolla, MO 65409-1060

http://www.ece.umr.edu/courses/cpe214

## Functional Diagram




## Pin Configurations




Rev 2: 12/19/2001-jjp

# Xilinx XC4005XL VGA Controller

## Pin Descriptions

| PIN Name | FUNCTION |
|---|---|
| data(7:0) | Data input to character framebuffer. The lower 5 bits contain the character code and the upper 3 bits contain the color code. |
| address(15:0) | Address input to the character framebuffer. The device responds only to addresses in the range FE00-FF80. |
| we | Active low write enable. Clocks data into the framebuffer. |
| clk | 12MHz externally applied clock. Drives the VGA controller and the framebuffer read/write logic. |
| Hsync | Output to VGA monitor Hsync pin. Signals the monitor to move the electron beam to the next scan line. |
| Vsync | Output to VGA monitor Vsync pin. Signals the monitor to move the electron beam to the top of the screen. |
| video | Video data output to VGA monitor. Determines the brightness of the current pixel. |
| dataout(7:0) | Framebuffer contents. Output of the framebuffer contents selected by the address lines. Undefined if the device is not selected. |
| sel | Output of address decoder. Output is high if the address pins are between FE00 and FFFF. |

## Detailed Description

### Controller Operation

This Xilinx XC4005XL VGA Controller uses a 12MHz clock to generate timing and data signals to drive a standard VGA monitor. It contains address decoding logic and a flat 32x12 framebuffer of which 16x8 is available for use. The address and data lines are used to write characters into the framebuffer, and the dataout lines can be used to read characters back.

The write enable line selects the device for writing into the framebuffer. The sel line is a tap of the internal address decoder. It is active when the address lines are between FE00 and FFFF.

### VGA Monitor Output

The Hsync, Vsync, and video pins comprise the output to a VGA monitor. Hsync is active low and is asserted for 3.77us every 31.77us. Vsync is active low and is asserted for .06ms every 1.667ms. video is a logic level output that drives the pixel values on the VGA monitor. A high logic level produces a white dot, while a low level produces black.

## Microprocessor Interface

### Writing

To write to the framebuffer, the address of the character to be written must be selected. See Figure 1 for the mapping between framebuffer locations and screen positions. Also the code for the character must be

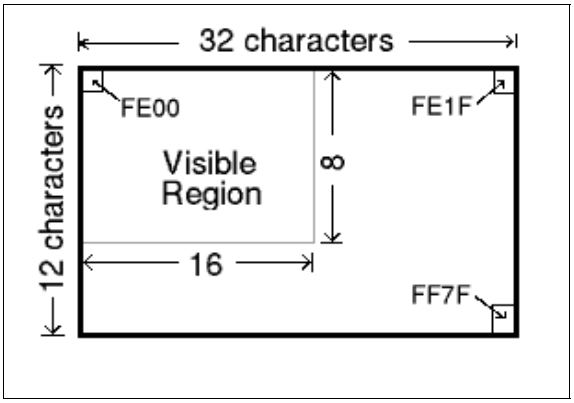



*Figure 1: Screen Configuration*

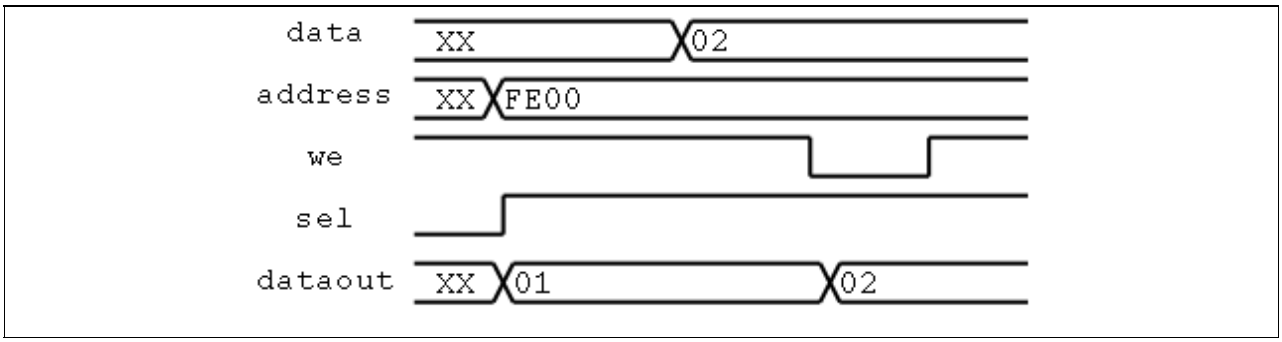



*Figure 2: Data Read/Write Sequence*

presented at the data lines. A falling edge on we then clocks this data into the framebuffer.

**Reading**

The value of the currently selected address is always present at the dataout pins. To utilize this ouptut on a data bus the sel pin can be used to drive tri-state buffers.

**Clock**

A 12MHz CMOS level clock should be applied to the clk pin. The timing for Hsync and Vsync is derived from this clock, so deviations from this frequency may damage fixed frequency monitors.

**Data Format**

The 8 bit word for each character is composed of a 3 bit color code, and a 5 bit character code. The characters are represented by 0-25, where A=0 and Z=25. The codes 26-32 are all blanks. The color bits are reserved for future use and are not implemented in this version.

**Table 1: Data Format**

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | R | G | B | D4 | D3 | D2 | D1 | D0 |

R,G,B => Reserved

D4-0 => Character Code

A-Z = 0-25

<blank> = 26-31

## Applications Information

**Data Bus**

The VGA controller can be directly interfaced to any microprocessor or microcontroller with a 16 bit address and 8 bit data bus. If the read functionality of the framebuffer is to be used, tri-state buffers must be used to isolate the dataout lines from the data bus when the part is not selected. These must be supplied either as logic on the FPGA or externally. They can be driven from the sel output, as it is the device's internal select line. See Figure 2 for a sample application.

**Video Interface**

The video output should be connected to all three RGB inputs of the VGA monitor. Hsync and Vsync outputs should be connected to their corresponding inputs.

**Sample Application**

The sample application shown in Figure 3 utilizes an 8051 microcontroller to drive the VGA controller in a read/write mode. The lower eight address bits are latched by a discrete latch. we is connected to WR/ of the 8051 to trigger a framebuffer write upon external memory access. The AND2B1 gate enables the dataout tristate buffer whenever the device is selected and the 8051's RD/ line is active.

**XESS40 Board**

When used as a part of the XESS40 board no modifications should need to be made, however the video output pin should be connected to all six available RGB inputs. The XESS40 board provides for two brightness levels of each color, however since

# Xilinx XC4005XL VGA Controller

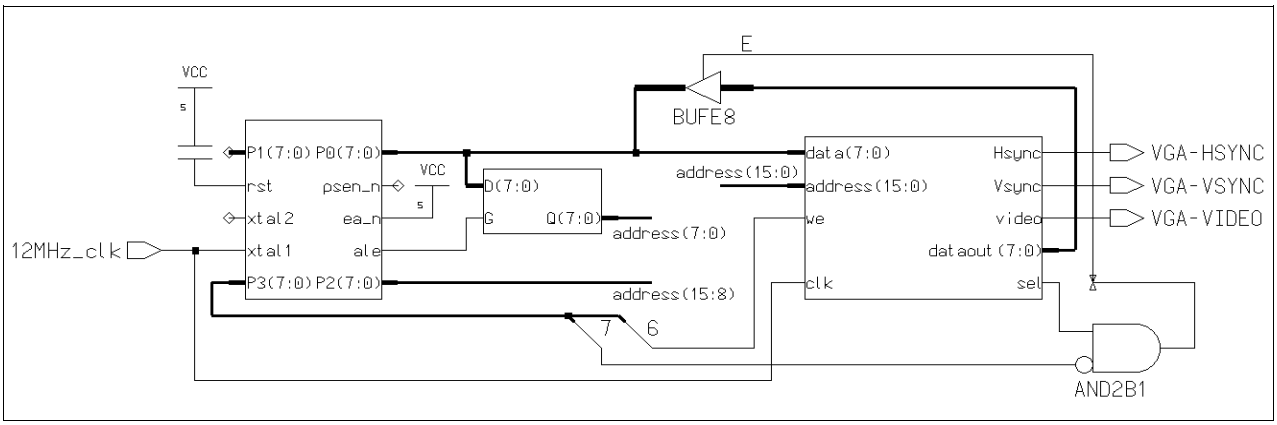



*Figure 3: Sample Application using 8051*

this is a monochrome controller they are not used independently. Any application in the XESS40 board in which a ROMless 8051 variant is used will also have to include logic to latch the lower address bits and logic to select the SRAM over some part of the address space.

## Porting Concerns

The VGA controller was designed to run in a Xilinx XC4005XL FPGA. It is designed as part schematic, part VHDL with schematic on top. There are two areas of concern when running on a different device. First the timing unit is constructed as as a VHDL model, so therefore would need to be re-synthesized for another Xilinx architecture. This can be done with the following procedure:

1. Modify `vgasrc/timing.scr` and `vgasrc/debug.scr` to contain the correct architecture
2. Run the `build_vga` script

Secondly a minimum implementation that allows reading from the framebuffer requires 189 CLBs to implement. Alternate parts would have to have at least this amount of logic available.

When creating a .BIT file for this design, ngdbuild must be passed the `-sd` option with the directory the synthesized netlists. If using the included `xmake` script, this is done already.