EMC and Signal Integrity in High-speed Electronics

Li Er-Ping, PhD, IEEE Fellow
Advanced Electromagnetics and Electronic Systems Lab.
A*STAR, Institute of High Performance Computing (IHPC)
National University of Singapore
Erpingli@ieee.org
About Singapore
About Singapore

Physical
- Land area: 699 sq km
- Limited natural resources
- Geographical position
- Natural harbour

Population
- 1960: 1.60 million
- 2006: 4.7 million (including 800K expatriates and migrant workers)

Economy (GDP)
- 1960: $1.5 billion
- 2006: $134 billion
- Per capita: $35,000

Political Landmarks
- 1959: Self-government
- 1963: Merger in Federation of Malaysia
- 1965: Independence (separation from Malaysia)

Foreign Reserves
- 1963: S$1.2 billion
- 2005: S$193.6 billion
Outline

1. Introduction

2. High-speed Electronics
   - Key SI/EMC Issues
     - Transmission Line effects
     - Crosstalk
     - Simultaneous Switching Noise (SSN)
     - Radiated Emission
   - Design Considerations

3. Summary
Introduction

Trends in IC & Package Industry

More Dense

Higher Frequency

Complexity of Intel microprocessors

Number of Devices

1GIGA

100MEG

10MEG

1MEG

100K

10K

Year

1980

1985

1990

1995

2000

2005

16 bits

32 bits

64 bits

Pentium

Pentium II

Pentium III

Pentium IV

Itanium

Operating Frequency

10GHz

100MHz

10MHz

1GHz

Year

1983

1986

1989

1992

1995

1998

2001

2004

2007

2010

Microprocessors (Intel)

Microcontrollers (Freescale)

Source: INTEL
Packaging and System Integration
-- A Roadmap --

System Integration:
- Analog/Digital
- Photonic
- Displays
- MEMS
- Energy

Vertical system integration

Integration Density

Wafer Scale Processing / Packaging

Multiple Functional Layers

SiP with MEMS

Thin Chip Integration

Chip on Chip

WL-CSP + IPD

WL-CSP

FC-CSP

WB-CSP

3D-Systen

2D-Systen

Logistic

Consumer

Medical

Automotive

Telecom

Polymer Block

Source: Fraunhofer IZM

Source: ICCE

2006

2009

2012
Introduction

Complex System-on-Package (SOP) Structure

Reference: Georgia Institute of Technology, Packaging Research Center.
3 "I"

- **SI** (Signal Integrity)
- **PI** (Power Integrity)
- **EMI** (Electromagnetic Interference)

EMC is a very important issue for IC & package design.
High-Speed Design Challenges

- **Timing**
  - Meet setup/hold requirements
  - Path level delay management
  - Clock distribution and skew

- **Signal Integrity**
  - Reflections, ringing, overshoot, monotonicity
  - Crosstalk
  - Simultaneous switching noise

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Both Simulations are the Same 15 cm Line!
Transmission Lines

- 10ns Driver
  - Both driving the same load 15 cm away
  - Impedance discontinuity at the Receiver (open)

- 100ps Driver
EMC design becomes more and more important

If not properly take EMC-Design

– One circuit will disturb another
  • Causing the output signal distortion
  • Causing signal delay
  • Mulfunction
– One board works properly, but the assembly may not work properly
– One device works properly at lab, but may work properly after installed on real environment
SI/EMI Design Objectives

Signal Integrity
• Make it work reliably
• Signal quality
• Timing
• Crosswalk
• Power/ground noise
• ...

EMI
• Make it comply EMI requirements
• Shielding
• Grounding
• Filtering
• Noise isolation
• ....
Key SI Issues

Propagation Delay

Electrically long interconnect: finite length of the transmission line comparable to the operating wavelength
Key SI Issues

Attenuation of Signal

Attenuation of signal due to

- Ohmic loss --- finite conductivity, skin/proximity effect
- Conductance loss – lossy substrate
Key SI Issues

Attenuation of Signal

**Skin effects:**
At high frequencies, current concentrated at the surface of the conductor.

\[
\delta_s = \sqrt{\frac{\rho}{\pi \mu f}}
\]

Resistance increases as square root of frequency!
Key SI Issues

Ringing & Reflection due to

Discontinuity in characteristic impedance of transmission lines

\[ Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad \Rightarrow \quad Z_0|_{\text{lossless}} = \sqrt{\frac{L}{C}} \]

# Structure related: bend, stub, etc.

# Transitions in transmission lines: Microstrip to stripline transition; vias

Discontinuity \(\rightarrow\) Reflection \(\rightarrow\) Ringing

High-order Harmonics
Key SI Issues

Ringing & Reflection due to Impedance Mismatch

Circuits’ Impedance \(\neq\) Transmission Line’s Impedance (Mismatching)

\(\rightarrow\) Multireflection \(\rightarrow\) Ringing
Key SI Issues

Crosstalk

Coupling path:

- Common-impedance (ground impedance)
- Electric field coupling (capacitive)
- Magnetic field coupling (inductive)
Crosstalk

Mutual Capacitance --- $C_M$

&

Mutual Inductance --- $L_M$

$C_M$ — The coupling of two conductors via the electric field.

$$I_{\text{noise},C_m} = C_m \frac{dV_{\text{driver}}}{dt}$$

$L_M$ — The current in one loop affects the second loop by means of the magnetic field.

$$V_{\text{noise},L_m} = L_m \frac{dI_{\text{driver}}}{dt}$$
Key SI/EMC Issues

Crosstalk Induced Delay

The worst scenario for delay is when the victim and the aggressor signals switch in opposite directions
Key EMC Issues

Simultaneous Switching Noise (SSN)

Also known as ground bounce, power bounce or delta-I noise.

- Voltage noise appears when circuit draws currents from the power distribution network.
- These effects cause unwanted switching and slow performance.
- The problem is amplified when many circuits switch at the same time.
Key EMC Issues

Simultaneous Switching Noise Propagation along Power Distribution Network

- SSN coupling to other signal traces
- Produce emission from package
Key EMC Issues

Emission from Package

Emission sources

- Heat sink wire connected to PCB
- Edge/gap of power-ground plane

- For low frequency, can be simplified to be a dipole antenna.
- For high frequency & complex structures, emission analysis is more complex than SI analysis.
Design Considerations

Balance between all EMC issues

Every control method is frequency dependent.
Design Considerations

Return Vias/Shorting Vias/Decoupling cap

- Provide return current for active via, reduce SSN
- Prevent propagation of EM wave from noise
- Isolate the noise source
- But introduce resonance for higher frequency
Design Consideration
Minimizing Cross-talk

- **Cross-talk (Near and Far End Cross-talk)**
  - Example: Near End Cross-talk

\[ \frac{V_b}{V_a} = K_b = \frac{1}{4} \left( \frac{C_{ML}}{C_L} + \frac{L_{ML}}{L_L} \right) \]

where
- \( V_b \) = Maximum voltage on quiet line
- \( V_a \) = Maximum voltage on active line
- \( K_b \) = Backward coefficient
- \( C_{ML} \) = Mutual capacitance per length
- \( C_L \) = Capacitance per length of signal trace
- \( L_{ML} \) = Mutual inductance per length
- \( L_L \) = Inductance per length of signal trace

- Use 2D Field Solver to Extract L and C Matrices
  - L and C matrices contain all information about coupling of traces, from which all aspects of cross-talk can be analysed (e.g., SPICE equivalent circuit model can be built,...)
Minimizing Cross-talk

- **Cross-talk (Near and Far End Cross-talk)**
- **Example: Near End Cross Talk – Comparison between FR4, Thin and Thick Film Substrates**

<table>
<thead>
<tr>
<th>Organic Substrate</th>
<th>Thickfilm Substrate</th>
<th>Thinfilm Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>FR4</td>
<td>Al2O3 Ceramic (96%)</td>
<td>Al2O3 Ceramic (99%)</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>4.20</td>
<td>9.2</td>
</tr>
<tr>
<td>$\tan\delta$</td>
<td>0.007</td>
<td>0.0023</td>
</tr>
</tbody>
</table>

5 % of noise margin allocated to cross-talk

Use substrate with lower dielectric constant

Space btw conductors must be at least 2W to keep $K_b$ less than or equal 2%
Minimizing Cross-talk

Via-to-via crosstalk

- Provide adjacent return/shorting via.

Minimizing Cross-talk-vias

- **Use Interplane Vias to Shield Sensitive Signal Paths**

a) 1 interplane via beside each signal via and no interplane via between signal vias

b) 1 interplane via beside each signal via and 1 interplane via between signal vias

c) 3 interplane vias beside each signal via and 1 interplane via between signal vias

- Cancellation of magnetic field leads to a reduction in cross-talk between the signal vias

I. Nidp, EPTC, 2005, Singapore
Minimizing Cross-talk-Vias

Cross-talk is reduced if three interplane vias are used to shield aggressor and one interplane via is placed between aggressor and victim.

Simulated Mutual Inductance

<table>
<thead>
<tr>
<th></th>
<th>(a)</th>
<th>(b)</th>
<th>(c)</th>
</tr>
</thead>
<tbody>
<tr>
<td>9pH</td>
<td>4pH</td>
<td>2pH</td>
<td></td>
</tr>
</tbody>
</table>
Design Considerations

Impedance Matching

- Match discontinuities:
  - Microstrip<-->Stripline
  - Wire bond<-->Signal Trace
  - PCB Trace<-->Cable

In general, Use blind and buried vias to cause less reflection comparing to the through-hole vias

(But some time is not true, depends on the structures, let’s examine)
Minimizing Reflections

- Comparison of Buried and Through-Hole Vias (ECPWG- ECPWG transition)
- Both vias were used to connect two 50 Ω traces in layers 2 and 3

<table>
<thead>
<tr>
<th></th>
<th>L/H</th>
<th>C/F</th>
<th>Z/Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buried via</td>
<td>1.0E-10</td>
<td>1.7E-13</td>
<td>24.9</td>
</tr>
<tr>
<td>Through-hole via</td>
<td>1.5E-10</td>
<td>1.1E-13</td>
<td>36.5</td>
</tr>
</tbody>
</table>

Through –hole via impedance is more close to the load 50 Ω, impedance match is better than buried via.

Ref: I. Nidp, EPTC, 2004, Singapore
Minimizing Reflections

To adjust the Pad/Hole Ratio for Capacitive Vias, also could minimize the reflections.

Smaller pad/hole ratio (smaller annular ring) leads to an increase in $Z_{via}$, thus reducing the reflections.

Larger distance btw via and reference, less reflection.
Minimizing Reflections

- Effects of bends when no other discontinuity is present along signal path

90° bend
Chamfered 90° bend
45° bend
Uniform trace

![Graphs showing S11 and S12 parameters for different bends and traces.]

- 45° bend
- 800 µm long trace
- 90° bend
- Chamfered 90° bend
Minimizing Reflections

- Effects of bends when other discontinuities are present along signal path
  - Example: 2.4 mm long signal path within the substrate

- Above 10 GHz use less than four 90° bends to keep reflection < 10%
- Use only 45° whenever possible. Up to 15 GHz, six 45° bends can be used and <10% of signal will be reflected.
- Effects of at least four 45° bends on RF performance of complete path can be neglected.
- One through-hole via causes more reflection than four 90° bends above 10GHz. So concentrate on via design!!
Minimizing Reflections

**Design Recommendations**

- Use smaller pad/hole ratio
- Increase or decrease vertical distance between blind and buried via and the nearest reference plane(s) accordingly
- Eliminate pads at reference planes and/or logically increase the size of the clearance hole
- If possible, holes can be bored in the reference plane(s), directly above and/or underneath pads of buried and blind via pads
- Use smaller via dimensions whenever possible
- Use Interplane vias to control via inductance of signal vias

*These design measures must be implemented at the beginning of the development cycle*
Power Distribution Network & Decoupling

Physical Structure of a PDN for high performance Circuit

Physical Structure of a PDN for high performance Circuit

A simplified circuit model for PDN

\[ Z_{PDN} = \text{the impedance seen from the two terminals of the load.} \]

Power Distribution Network Noise Suppression Using Decoupling Capacitors (Decaps)

1) Four Decaps:

\[ C = 10 \text{ nF}, \quad ESL = 3 \text{ nH}, \quad ESR = 0.2 \text{ Ohms} \]

Increasing the radius \( r \) of the decaps around port 1 will change the impedance \( Z_{21} \), but the impedance may increase or decrease due to exciting different resonant modes.

Fig. 5 Four decaps are added to the power-ground structure: (a) 3D view; (b) top view.

Fig. 16 Distribution of \( E_z \) field on the power plane at 2 GHz.
**PDN Noise Suppression Using Decoupling Capacitors (Decaps)**

2) **Eight Decaps:**

Adding more decaps may reduce the impedance level.

But it will also shift the resonant frequencies of the structure to a higher value.

3) **Add Both Local and Global Decaps**

Adding both local and global decaps may greatly reduce the impedance level.

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**Fig. 7** The transfer impedance of the structure with eight decaps.

**Fig. 10** The distribution of the local and global decaps.

**Fig. 11** Results of transfer impedance due to local and global decaps.
Summary

- Key SI (signal integrity)/EMC issues
  - **Transmission Line effects**: delay, ringing & reflections, impedance mismatch
  - **Crosstalk**: due to capacitive and inductive coupling; induced delay
  - **Simultaneous Switching Noise (SSN)**: Voltage noise appears when large number of circuits draws currents at the same time from power
  - **Radiated Emission**: radiation due to edge effect, cable, and current loop

- Balance between Different EMC Control Methods --- every Control Method is Frequency Dependent
EMC Cost

Available techniques and relative cost to solve noise problem

Design Phase  Testing Phase  Production Phase

techniques

cost

Equipment Development, Time scale
Thank You!