Power Integrity and EMC Design for High-speed Circuits Packages

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Outline

- Power Distribution Network (PDN)
- Mechanism of Power Noise
- Issues and Quantification of Power Noise
- Solutions of Suppressing Power Noise
  - Decoupling Capacitors
    - Power/ground planes (PKG, PCB)
    - Surface mounted capacitor (PCB, PKG)
    - Embedded capacitor (PKG)
    - On-chip capacitor (Chip)
  - Isolation slots
  - EBG structures
    - Electromagnetic Bandgap (EBG) Power Planes
    - Photonic Crystal Power Layer (PCPL)
- Conclusion
Trends for high-performance Electronics


<table>
<thead>
<tr>
<th>Year</th>
<th>Feature</th>
<th>$V_{dd}$</th>
<th>Chip Freq.</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>2007</td>
<td>68nm</td>
<td>1.1V</td>
<td>4.70GHz</td>
<td>189W</td>
</tr>
<tr>
<td>2010</td>
<td>45nm</td>
<td>1.0V</td>
<td>5.88GHz</td>
<td>198W</td>
</tr>
<tr>
<td>2013</td>
<td>32nm</td>
<td>0.9V</td>
<td>7.34GHz</td>
<td>198W</td>
</tr>
<tr>
<td>2016</td>
<td>22nm</td>
<td>0.8V</td>
<td>9.18GHz</td>
<td>198W</td>
</tr>
<tr>
<td>2019</td>
<td>16nm</td>
<td>0.7V</td>
<td>11.48GHz</td>
<td>198W</td>
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</table>

**Low voltage**  **High speed**
Power Distribution Network (PDN)

An Electronic System
Power Distribution Network (PDN)

Chip Level

- Decoupling capacitor on PCB
- Decoupling capacitor on Package
- Wire bonding
- Flip chip
- Ball Bonding
- VRM

On-chip capacitor
P/G Grids
Interconnects
Pads
Power Distribution Network (PDN)
interconnects for Chip-PKG-PCB

- Decoupling capacitor on Package
- Flip chip
- Ball Bonding
- Chip
- Wire bonding

Fine pitch: 50-100µm
Line length: 100-200 mil

Bump pitch: 100–300µm
BGA Ball pitch: 0.5mm – 1mm
Power Distribution Network (PDN)  
**decoupling capacitors**

**Equivalent capacitor circuit**

\[
\text{Impedance} = j\omega ES + \frac{1}{j\omega C} + ESR
\]

- Ground
- Power
- Decoupling capacitor on PCB
- Decoupling capacitor on Package
- Chip
- Flip chip
- Ball Bonding
- Chip Bonding
- VRM

**External electrode**

**Ceramics**

**Internal electrode**
Power Distribution Network (PDN)

PWR/GND Planes

- Decoupling capacitor on Package
- Flip chip
- Wire bonding
- Ball Bonding
- Chip
- Ground
- Power
- VRM
Power Distribution Network (PDN)

Equivalent Model

- Decoupling capacitor on Package
- Flip chip
- Ball Bonding
- Wire bonding
- VRM
- Ground
- Power

Components:
- VRM
- PCB
- Ball Bonding
- PKG P/G
- Wire bonding

- Bulk Capacitor near VRM
- SMT C on PCB
- SMT C on PKG
- On-chip C

VRM P/G Network
Ball Bonding
PKG P/G Network
wire Bonding

Chip
Mechanism of the Power Noise: low-speed view

P/G noise arises whenever a changing current flow through the total inductance of the return path.

\[ I_{cut} = C_L \frac{dV_{in}}{dt} \]

switching voltage

 transient current \((\Delta I \text{ noise})\)
Mechanism of the GBN: high-speed view
A 4-layer PCB

Signal in

Layer 1

Layer 2

Layer 3

Layer 4

Via
P/GBN Coupling through Via Transition ($S_{21}$)

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>0.72</th>
<th>0.906</th>
<th>1.44</th>
<th>1.706</th>
<th>2.31</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{21}$ (dB)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Perfect Plane**
- **FDTD Modeling**
- **Measurement**

**Dimensions**
- Port 1: (4 cm, 4 cm)
- Port 2: (1.5 cm, 6 cm)
- Via Trace: (3 cm, 1 cm)
- Power: 50 ohm
- Ground Trace: 50 ohm
- Noise Source: d = 20 mils
- Via: d = 40 mils
- Distance: 20 mils

**Mode**
- $m,n = 1,0$
- $m,n = 0,1$
- $m,n = 2,0$
- $m,n = 2,1$
- $m,n = 2,2$
Issues caused by power noise

Signal Integrity Issues
- Jitter, Skew
- Crosstalk
- Eye width/height

Noise current to RF transceiver

Decoupling Capacitors
- Digital IC die
- Signal via
- Analog IC die

RF transceiver

Radiated Emission

EMI Issue

RFI Issues
- RF sensitivity

EMC DL 2008
Example of signal integrity issues

![Diagram showing signal integrity issues]

- **Package P/N network**
- **Decoupling C on chip**
  - Input
  - VSS
  - Out
  - Remove Decoupling C on chip

**Out-VSS (V)**

**Out-VSS (V)**
Example of EMI Issues

radiation of reference board

- excitation amplitude: 20mV
- excitation location: (6cm, 6cm)

|\( |E_z| \text{ at 3m(dBuV/m)} \) | Frequency(GHz) |
|---|---|
| simulation | measurement |

- \( T_{M0}^0 \)
- \( T_{M1}^0 \)
- \( T_{M1}^1 \)
- \( T_{M2}^0 \)
- \( T_{M2}^1 \)
- \( T_{M3}^1 \)
- \( T_{M4}^1 \)

- 0.2
- 0.4
- 0.6
- 0.8
- 1
- 1.2
- 1.4
- 1.6
- 1.8
- 2

30MHz~2GHz
Example of RFI Issues

VCO’s performance is affected by power noise
Quantification of Power Noise: Z parameter

[Diagram showing PDN components: VRM, Bulk Capacitor near VRM, Decoupling C on PCB, Decoupling C on package, Decoupling C on chip, P/G Network, Ball Bonding, wire Bonding, I2, V2, V1, I1, I2 to I1, V2 to V1]

\[
\begin{bmatrix}
V_1 \\
V_2
\end{bmatrix} = \begin{bmatrix}
Z_{11} & Z_{12} \\
Z_{21} & Z_{22}
\end{bmatrix} \times \begin{bmatrix}
I_1 \\
I_2
\end{bmatrix}
\]

\[Z_{11} = \frac{V_1}{I_1} \text{ (Port 2 open)}\]
\[Z_{21} = \frac{V_2}{I_1} \text{ (Port 2 open)}\]

**PDN Design:**

- Lower \(Z_{11}\) (Target impedance)
- Lower \(Z_{21}\)
Measurement of PDN Impedance

Z-parameter and S-parameters

Transfer impedance

\[ Z_{21} = Z_0 \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \]

Assume

\[ S_{11} \approx S_{22} \approx -1 \quad \text{(Low impedance PDN)} \]
\[ S_{12} \cdot S_{21} \approx 0, \quad Z_0 = 50\Omega \]

⇒ \[ Z_{21} \approx 25 \cdot S_{21} \]

Self impedance: (two probes are very close)

\[ Z_{11} = \frac{Z_0}{2} \frac{S_{21}}{1 - S_{21}} \quad \Rightarrow \quad Z_{11} \approx 25 \cdot S_{21} \quad \text{(assume } S_{21} \ll 1) \]
Capacitance
Given by VRM

Decoupling capacitor of package

Resonance

Inductance by
- ESL of discrete capacitor
- Power/ground trace

Frequency (Hz)

1006
1007
1008
1009

10
0.1

Mag (Z(1,1))

Target impedance

Antiresonance

Resonance

Antiresonance

Inductance by
- Power/Ground Plane
- Package via

VRM

Bulk Capacitor near VRM

Decoupling C on PCB

Decoupling C on package

Decoupling C on chip

PCB

P/G Network

Ball Bonding

package

wire

Boding

P/G Network

[1]

[2]

[3]

[4]
Power/Ground Planes

A Test Sample

PCB

Die

package

Decoupling capacitor

port1

port2

4 cm

8 cm

10 cm
Power/Ground Planes

Measurement setup

- VNA
- Probe
- Power ring
- Power via
- Ground ring
- Signal
- Ground
- PCB
- Package
- 0.4 mm
- 10 cm
- 8 cm

Port 1
Ground ring
Die pad
Port 2
Ground plane
Power plane
0.7mm
100um
150um
100um

NTU
National Taiwan University
EMC DL 2008
Power/Ground Planes
Coupling between PKG and PCB

Measurement Results

The SSN could be magnified by the interaction of these two cavities and degrades the power integrity of the packaged integrated circuits.

The PDS behavior of combining the package and PCB is similar to that of considering only the package.

Power/Ground Planes

Cavity resonance

900 MHz
$\text{TM}_{10}$

1.1GHz
$\text{TM}_{11}$
SMT Capacitors

Design Question?

- Locations?
- Numbers?
- Values?
SMT Decoupling Capacitors

Capacitors placed either on Package or PCB

- 52 capacitors on package
- 63 capacitors on PCB
- Capacitance: 100 nF
- ESR: 0.04 ohm, ESL: 0.63 nH
The additional resonance peak worsens the PDN performance.

Decoupling capacitors placed on package have better performance.

The behavior of the PDN is similar to that with the caps mounted on the package.
SMT Decoupling Capacitors

Capacitors Number Effect

With increasing the number of decoupling capacitors, the peaks move to higher frequency and their magnitude become smaller.

C:100nF (on Package)
ESR:0.04ohm
ESL:0.63nH
SMT Decoupling Capacitors

Capacitance value Effect

**100nF capacitors** have better performance to reduce noise at low frequency.

**100pF capacitors** have better performance at higher frequency. At low frequency, the capacitors can reduce noise about 8 dB.
Embedded Capacitor

Embedded Capacitor Properties:

Dk (10kHz): 3000
Capacitance Density: 1.0 nF/mm²
thickness: 20-30 μm
Cu Electrode thickness: 5-7μm
Caps location
Impedance measurement

Good capacitor is seen below SRF.

SRF is in the several MHz range due to large ESL of the connecting vias.

The bandwidth could be enhanced by designing the capacitor closer to the surface of the package.
Isolation by etched slot with bridges

Schematic diagram of the Isolated and Bridged Power Planes in Four Layers PCB Circuits
Isolation slots with bridge

Reference board

Moat-bridged board

Excited location: port 2

Dotted line: measurement
Solid line: 3D-FDTD

Frequency (GHz)

|S_{12}| (dB)
Isolation by etched slot with bridge  
(P/G Noise of the bridged board)


Fundamentals for EBG Structure

**circuit view**

\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{unit cell}} = \begin{bmatrix}
\cos \frac{\theta}{2} & jZ_0 \sin \frac{\theta}{2} \\
jY_0 \sin \frac{\theta}{2} & \cos \frac{\theta}{2}
\end{bmatrix} \begin{bmatrix}
1 & jX \\
0 & 1
\end{bmatrix} \begin{bmatrix}
\cos \frac{\theta}{2} & jZ_0 \sin \frac{\theta}{2} \\
jY_0 \sin \frac{\theta}{2} & \cos \frac{\theta}{2}
\end{bmatrix}
\]

\[
= \begin{bmatrix}
\cos \theta & jX \cos^2 \frac{\theta}{2} \\
Y_0 \sin \theta (1 + j) - jXY_0^2 \sin^2 \frac{\theta}{2} & \cos \theta - \frac{X}{2} Y_0 \sin \theta
\end{bmatrix}
\]
**Fundamentals for EBG Structure**

**circuit view**

- **Case 1**: (Pass Band)
  \[ \alpha = 0 \quad \beta \neq 0, \pi \]
  \[ \cos \beta d = \cos \theta - \frac{X}{2} Z_0 \sin \theta \]
  \[ |\cos \theta - \frac{X}{2} Z_0 \sin \theta| \leq 1 \]

- **Case 2**: (Stop Band)
  \[ \alpha \neq 0 \quad \beta = 0, \pi \]
  \[ \cosh \alpha d = \left| \cos \theta - \frac{X}{2} Z_0 \sin \theta \right| \geq 1 \]
Fundamentals for EBG/ PBG Structure

wave view
Fundamentals for EBG/ PBG Structure

wave view

1D example (no DK contrast)
Fundamentals for EBG/ PBG Structure

wave view

- DK1 = 15
- DK2 = 13

- DK1 = 15
- DK2 = 2.2

Normalized Frequency [ka/2π]

Photonic Bandgap

Wave vector [ka/2π]
Fundamentals for EBG/ PBG Structure

wave view
High-impedance Surface (mush-room) concept

\[
Z_0, \beta \\
\begin{array}{c}
\cdots \\
\end{array}
\begin{array}{c}
L_v \\
C_p
\end{array}
\begin{array}{c}
Z_0, \beta \\
\cdots
\end{array}
\]

\[
f_{\text{start}} = \frac{1}{2\pi \sqrt{C_p \left[ L_v + \frac{\mu_0 h}{4} \right]}}
\]

High-impedance Surface (mush-room)

bandwidth enhancement

Cascaded HIS: to improve the bandwidth

High-impedance Surface (mush-room) bandwidth enhancement

(c) Double-Stacked HIS

(d) Spiral HIS


Electromagnetic Bandgap (EBG) Power Planes

- Broadband suppression of the P/GBN
- Low EMI caused by the P/GBN
- Isotropically elimination of the P/GBN
- Very low cost

1D-equivalent circuit model

\[ \varepsilon_r = 4.3 \]

\[ \begin{align*}
2n - 2 & \quad 2n - 1 & \quad 2n & \quad 2n + 1 & \quad 2n + 2 & \quad 2n + 3 \\
Q_{2n-2} & \quad Q_{2n-1} & \quad Q_{2n} & \quad Q_{2n+1} & \quad Q_{2n+2} & \quad Q_{2n+3}
\end{align*} \]
P/GBN suppression— Frequency domain

![Diagram showing P/GBN suppression in the frequency domain.](image)

- Reference board
- 9-cell LPC-EBG board

- Excited location: (45mm, 45mm)
- Received location: (15mm, 75mm)

- Solid line: 2D-FDTD
- Dotted line: measurement

- |S21| (dB) vs. Frequency (GHz)
P/GBN suppression—Time domain (3D-FDTD)

There is over 35% of the GBN suppression rate by LPC-EBG power plane design.
P/GBN suppression — Time domain (measurement)

Excitation source (2.25GHz clock with amplitude of ±125mV)

9cell-EBG board (peak to peak 7mV)
EMI elimination
— LPC-EBG structure

Reference board

9-cell LPC-EBG board

Excited amplitude: 20mV
Excited location: (45mm, 45mm)

EMI at 3m
Solid line: 3D-FDTD
Dotted line: measurement
Impact on SI — Traces referring to EBG planes

MEO=363mV MEW=370ps
Reference board (with solid power/ground planes)
MEO=440mV MEW=388ps

L-bridged EBG Power Plane

Power plane

Ground plane

Substrate

Reference board

Power plane

Ground plane

Substrate

L-bridged EBG board

L-bridged EBG geometrical parameters

Power plane

Ground plane

90mm x 90mm x 0.4mm

Unit Cell

\[ \begin{align*}
  a &= 30 \text{ mm} \\
  w &= 6.65 \text{ mm} \\
  g_1 &= 0.1 \text{ mm} \\
  g_2 &= 0.2 \text{ mm} \\
  g_3 &= 0.75 \text{ mm} \\
  l &= 15.2 \text{ mm}
\end{align*} \]
Wideband suppression

![Graph showing wideband suppression with different curves for FDTD, FEM, and Measurement, indicating reference and L-bridged conditions.](image-url)
EMI performance

![Graph showing EMI performance](image-url)

- Frequency (GHz)
  - 0.05 to 2.55 GHz
- Ez at 3m (dBuv/m)
  - Measurement
  - Reference
  - L-bridged
EMS measurement setup

- According to IEC61000-4-3
  - Modulation: CW
  - Frequency Range: 80 MHz ~ 3 GHz
  - Dwell time: 1 sec
  - Frequency step: 2%
  - Electric field intensity: 3 V/m

EMS frequency-domain response

solid line: simulation
dash line: measurement

EBG board
Reference board

mV

0 2 4 6 8 10 12 14

Frequency(GHz)

0 0.5 1 1.5 2 2.5 3

EBG board
Reference board
Photonic Crystal Power Layer (PCPL)

Multilayer PCB substrate

The geometry of the PCPL

High-DK material

$\varepsilon_r = 110$

$Q = 1003$ (f = 7GHz)
Dispersion diagram for the PCPL

In this diagram, the bandgap is represented by frequency range in which there is no propagating mode for any propagation vectors.

The dots -- FDTD method
The solid lines -- MIT photonic band tool

SL-PCPL

Square lattice

Frequency (GHz)
P/GBN suppression – Frequency domain

Bandgaps

\[ \varepsilon_{\text{eff}} = A_r \varepsilon_r + (1-A_r) \varepsilon_0 \]

\[ \varepsilon_{\text{eff}} = 10.348 \]

\[ C_{\text{eff}} = 716\text{pF} \]
P/GBN suppression – Time domain

The waveform of the excitation source 10Gbps and amplitude ±125 mV

Square lattice

SSN can be reduced about 91%
Signal Integrity Performance

Input signal:
2^23-1 pseudo random bit sequence (PRBS), nonreturn to zero (NRZ), coded at 10GHz.

Bit rate: 10 Gbps
Amplitude: 500 mv
Edge rate: 35 ps
Eye Pattern Simulation (TL-PCPL)

MEO = 245 mV, MEW = 72 ps

Ref brd

MEO = 292 mV, MEW = 85 ps

PCPL

MEO \rightarrow \text{Maximum Eye Open}

MEW \rightarrow \text{Maximum Eye Width}
EMI elimination — PCPL structure

At the frequency range of the bandgap, the radiation resulted from the SSN is significantly suppressed with over 30dB reduction.
Gap map for PCPL structure

Area of maximum bandwidth for the first bandgap

The substrate almost filled with high-DK rods

For the application, we need the broad stopband at low frequency. Therefore, there is design tradeoff between the bandwidth and the center frequency for the PCPL structure.

Gap map of the PCPL structure for different dielectric constant

- The bandgap appears at smaller r/a for larger dielectric constant.
- The center frequency of the band at the same r/a is higher for the smaller dielectric constant.
Conclusion

• P/GBN is one of the key issues for designing high-speed digital circuit with good signal integrity (SI) and EMC performance.

• Several approaches to eliminate the P/GBN on the power delivery systems are investigated by both numerical simulations and experimental measurement.