Selective Laser Sintering of Multilayer, Multimaterial Circuit Components

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Abstract — Selective Laser Sintering (SLS) is presented for the creation of multilayer circuit components compatible with microwave frequencies. SLS is a one step process that uses a laser to pattern and fully sinter screen printable inks without the use of any high temperature post processing. For the first time, this process is demonstrated for multiple layers of material with varying properties, such as metals and dielectrics. Sequentially sintering conventional thick film materials is used to create functional layers, both conductive and dielectric, in a layer by layer fashion, forming metal-insulator-metal (MIM) capacitors and spiral inductors on soda-lime glass.

Index Terms — Laser materials-processing applications, thick film capacitors, thick film inductors.

I. INTRODUCTION

Screen printing thick film inks is a well established technology with an extensive supply of different material inks, such as conductive, dielectric and resistive. Conventional thick film processing requires 850°C firing temperature in order to functionalize the patterns, by sintering the materials to near full density. This limits the choice of substrates to high temperature substrates such as ceramics and quartz.

Thick film inks can also be precisely deposited on a substrate using direct writing (DW) processes. The major benefit of the DW approach is that there is no need for any physical screens or masks; this is a major advantage for rapid prototyping and small batch manufacturing. In addition, the absence of a screen permits that fabrication of smaller feature sizes than are obtainable using screen printing.

Well known DW techniques include: Matrix Assisted Pulsed Laser Evaporation Direct Write (MAPLE-DW), ink jet printing, and MicroPen™ dispensing [1]. The first technique uses a laser to transfer unfired material from a sacrificial target onto the intended substrate. The other two methods dispense material in droplets from a nozzle onto a substrate. The disadvantage to these DW techniques is that they all require thermal post processing in order to sinter the components to acquire the desired material properties, thus the choice of substrates is still limited by the firing profile. Multilayer circuit components have been demonstrated using all of the mentioned techniques [2]-[4]. The substrate materials that can be utilized by these are limited by the temperature of the post processing firing steps.

Laser sintering patterns deposited by other DW techniques has been proposed in [1]. Alternatively, laser sintering can be used to not only functionalize the component but also generate the pattern. This integrated approach, referred to as Selective Laser Sintering (SLS) has been previously demonstrated using a continuous wave (CW) infrared (IR) laser to fabricate components using thick film conductive inks [5]-[6]. Not only does SLS have all the benefits of standard DW techniques, it does not require the patterns and substrate to be post processed at high temperatures. The heating is done locally; allowing the heat to diffuse laterally to the surrounding ink, thus minimizing the heat transfer to the substrate. This enables the use of low temperature substrates. Microwave resonators and high frequency patch antennas on soda-lime glass, quartz, and FR4 have been demonstrated [5]-[6]. Neither the soda-lime glass nor the FR4 will survive the traditional firing profile, and therefore the metal application process has been verified to be very flexible in its application space for depositing.

In this paper, the SLS process is extended to sinter multilayer circuit components with both metal and dielectric layers, such as capacitors and inductors. This is significant because this allows the fabrication of complete circuits on low temperature substrates, by combining these components, without any additional thermal processing.

II. MULTILAYER FABRICATION

The SLS setup and process has already been described for single layer, metal only circuit components, such as antennas and resonators on a microwave substrate [5]-[6]. Multilayer component fabrication is more involved and requires additional steps that are detailed in this paper.

In order to selectively laser sinter a Metal-Insulator-Metal (MIM) parallel plate capacitor, the dielectric must be sintered between two sintered conductor electrodes. A wide variety of screen printable dielectric materials are available, ranging from low dielectric constants to greater than 3,000. For the first demonstration of the concept, the capacitor multilayer DuPont QM44 as the dielectric layer. The specified dielectric constant from the manufacturer is given to be εr = 8. The conductive ink used is a commercial silver based ink, QS300 from DuPont. The specified sheet resistance for QS300 is 4.5 mΩ/square for a 10 μm thick trace, which corresponds to a conductivity σ of 2.2×10⁴ S/m. Both inks are designed to be fired at 850°C. The firing profile for traditional processing of these inks requires a dwell time of 2-3 minutes at that temperature.

Capacitors are fabricated on soda-lime glass, to demonstrate that the processing can be done on non-traditional thick film substrates, in several steps as shown in Fig. 1. Fig. 2 shows a
photograph of the final component. First the substrate is completely coated with the silver ink. The entire substrate is placed in a convection oven to drive off the organic components in the ink. This heating step takes place at 120°C which is below the damage threshold of the glass and most polymer substrates. The ink is simultaneously patterned and sintered by scanning the laser beam over it. The electromagnetic energy absorbed by the ink is converted to thermal energy. The laser acts as a heat source near the surface and generates a high temperature rise in the ink, sintering the functional particles together. This heating also produces a fusion bond between the ink and the substrate. The effects of the laser parameters on electrical performance are discussed in more detail in [5]. After patterning the unsintered ink is dissolved in methanol using an ultrasonic cleaner.

After the fabrication of the ground conductor the entire substrate is coated with dielectric ink. Thinner is added to the ink to reduce its viscosity and permit the coating of a thin conformal layer using a wire coater or a spray system. The ink is thinned so that a thin conformal coating can be applied using a wire coater or spray system. The application, drying and patterning, and cleaning steps are identical for the silver ink with the exception that the laser parameters for this ink are different because it has a different optical absorptivity and thermal diffusivity. This step can be repeated to build to a desired thickness for the dielectric layer. Two sets of capacitors are made using 5 and 6 layers of dielectric respectively. Each layer is roughly 7 µm thick. Multiple layers can be deposited very quickly because the time it takes to sinter each layer is on the order of 10 seconds. Since the heating is kept localized, there will be minimal damage to the substrate due to repeated thermal cycling. Finally, the top conductor is patterned using the same laser parameters and procedure as used for the bottom conductor.

Fig. 3 shows a scanning electron microscope (SEM) image of the top metal path from the dielectric down to the glass substrate. The figure demonstrates that there is a smooth transition from the top of the dielectric, along the sidewall and all the way down to the glass substrate.

A common failure mode in most multilayer, multimaterial circuit components is shorting the two electrodes through the dielectric via pinholes. To prevent pinholes, several layers of
dielectric are usually sintered sequentially, filling any possible holes in the layer. This results in a thicker dielectric and will decrease the capacitance available for a given geometry. Another remedy is to change the settling time of the ink; this reduces the number of pinholes and voids. For SLS, the laser power and speed are additional variables that control the temperature profile within the ink. These parameters can be controlled so that the dielectric layer is heated above its melting point during processing causing it to flow and fill in any voids. The laser parameters determine the thermal profile, controlling the sintering process, and thus the possible formation of pinholes during the sintering process.

The multilayer fabrication has the same potential failure modes found in sintered conductive patterns [5]. Peeling and flaking is observed due to poor adhesion if the temperature is insufficient. Damage to the glass substrate is observed if the heat generated is too high. In order to achieve the specified properties for the dielectric and conductive inks, the heat generated must be balanced to burn out all the remaining organic binder and fusing the particles together to the substrate, while not excessively heating the substrate.

III. EXPERIMENTAL RESULTS

The fabricated capacitors are measured using HP 4284A LCR meter. All the capacitors are measured and the average capacitance is 12.53 pF and 9.62 pF for the first and second set respectively, both measurement sets have a standard deviation of 0.1 pF. Table 1 contains a complete listing of the results.

In order to calculate the expected values using the parallel plate equation, the dielectric thickness is measured using an Alpha-Step® IQ surface profiler. The measured values are within 10% of the expected values; this indicates that the quality of the dielectric is compatible with that from the standard firing profile.

Fig. 4 shows three cross-sectional profiles at different positions in the capacitor. The bottom electrode is the same height as the feed conductor. The figure shows some roughness in the topology of the dielectric layer. This may be attributable to melting and reflow during the sintering process. This phenomenon can also be observed in Fig. 3. The bottom electrode and substrate were not damaged during the application and sintering of the dielectric. Melting of the glass constituents in the ink is necessary to form a fusion bond with the substrate and/or underlying material.

![Cross-sectional profiles of fabricated capacitor structure.](image)

The capability of the process to fabricate other passive components, such as high-frequency transmission lines and inductors is also of interest. In order to demonstrate this, a coplanar waveguide (CPW) transmission lines were fabricated on soda-lime glass using QS300. Fig. 5 shows one of the fabricated geometries. This CPW line has a 461 μm center conductor and 85 μm gaps.

![Selectively laser sintered CPW lines with a 461 μm center conductor and 85 μm gaps.](image)

The CPW lines are measured up to 26 GHz to investigate the high frequency performance. In Fig. 6 the S-parameters of the CPW line in Fig. 5 are plotted along with simulated results from Advanced System Design (ADS). The CPW lines match simulation very well and the exhibit a loss of around 2 dB at 26 GHz, this loss is predominately from the dielectric loss of the soda-lime glass. This corresponds to a loss of 0.219 dB/mm and is consistently observed for CPW lines with gap sizes down to 35 μm. This demonstrates that fine features with precision edges can be fabricated with sufficient accuracy that they exhibit a high level of agreement with values obtained from numerical simulation.

<table>
<thead>
<tr>
<th>Capacitor set #</th>
<th>Mean Measured Capacitance (pF)</th>
<th>Standard Deviation (pF)</th>
<th>Mean Calculated Capacitance (pF)</th>
<th>Mean Dielectric Thickness (μm)</th>
<th>Relative difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12.53</td>
<td>0.1027</td>
<td>12.99</td>
<td>35.25</td>
<td>3.54%</td>
</tr>
<tr>
<td>2</td>
<td>9.62</td>
<td>0.1099</td>
<td>10.60</td>
<td>43.17</td>
<td>9.28%</td>
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</tbody>
</table>
To demonstrate the flexibility of the multilayer process, it is utilized on an eleven turn spiral inductor to form the overpass from the center of the inductor to the output as shown in Fig. 7. Several layers of dielectric are sintered to form this overpass. The spiral metal layer is fabricated on the same substrate using QS300 for the metal layers. The measured low frequency inductance of this structure is 176 nH.

Fig. 7. Eleven turn spiral inductor with a dielectric overpass for the center conductor.