Dr. Dua

Electronics II

9/16/13

Single Stage Common Emitter Amplifier Project

The first project for Electronics II was to create a single stage common emitter BJT amplifier. The goal was to choose an npn transistor with the spice model from Newark.com. The design for this circuit must be bias stable, include AC gain stability and emitter bypass capacitor. The maximum gain for an undistorted signal output is desired and suitable coupling capacitors that shape the lower frequency response. The calculations for the DC portion of the design are located in appendix 1. The data collected from the lab and calculations from that data after assembling the circuit designed in appendix 1, is located in appendix 2. The calculations for the coupling and bypass capacitors are located in appendix 3. The upper cutoff frequency calculations are in appendix 4. Finally in appendix 5 are the circuit diagrams Figure-1 is the DC portion of the circuit and Figure-2 is the entire finished circuit.

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were made in appendix-1

Now that all the resistor values are known, the circuit in appendix-4 was created in lab and the DC col . From the DC circuit Figu ced in the

circuit to find the gain. The signal was distorted initially, because the output was clipped. After pressing the -40d The output peak to pe circuit, using the equatio

The desig toff frequency of 50H ff frequency. The f toff frequencies were

After repl did not change the output. The lower cutoff frequency obtained in lab the was 21Hz, and the upper cutoff frequency 625kHz. Refer to the appendix 4 for the calculated upper cutoff frequency without changing the Rs value.

but it s resistar decreas upper c R_S has a huge effect on the upper cutoff frequency, it annihilates all the other resistances in the circuit.

There is a way to take control of the R_S value by adding a resistor in series with the function generator, if the added series resistor is much larger than R_S, then R_S is approximately equal to the resistance added. A 2kΩ resistor was added in series with the function generator as shown in figure – 2, and the new I_C, V_{CB}, and V_{EB} values were obtained. The β value and the

voltage across R_E remained the same. Using these values obtained in the lab the upper cut-off frequency could be calculated using the same formulas in appendix-4. The new calculated upper cutoff frequency was 232kHz and the recorded cutoff frequency in the lab was 159.6kHz, which is only 72.4kHz difference.

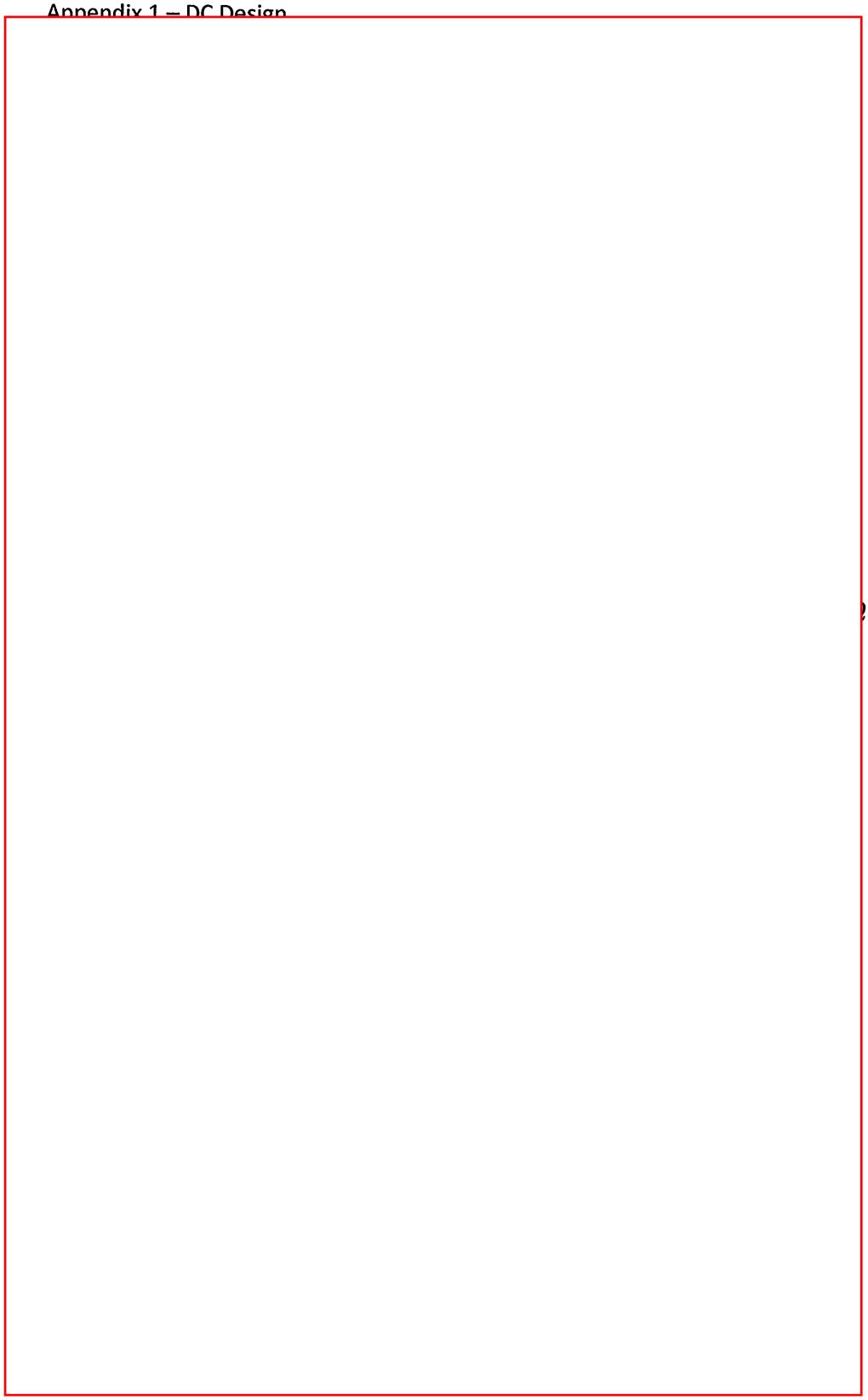
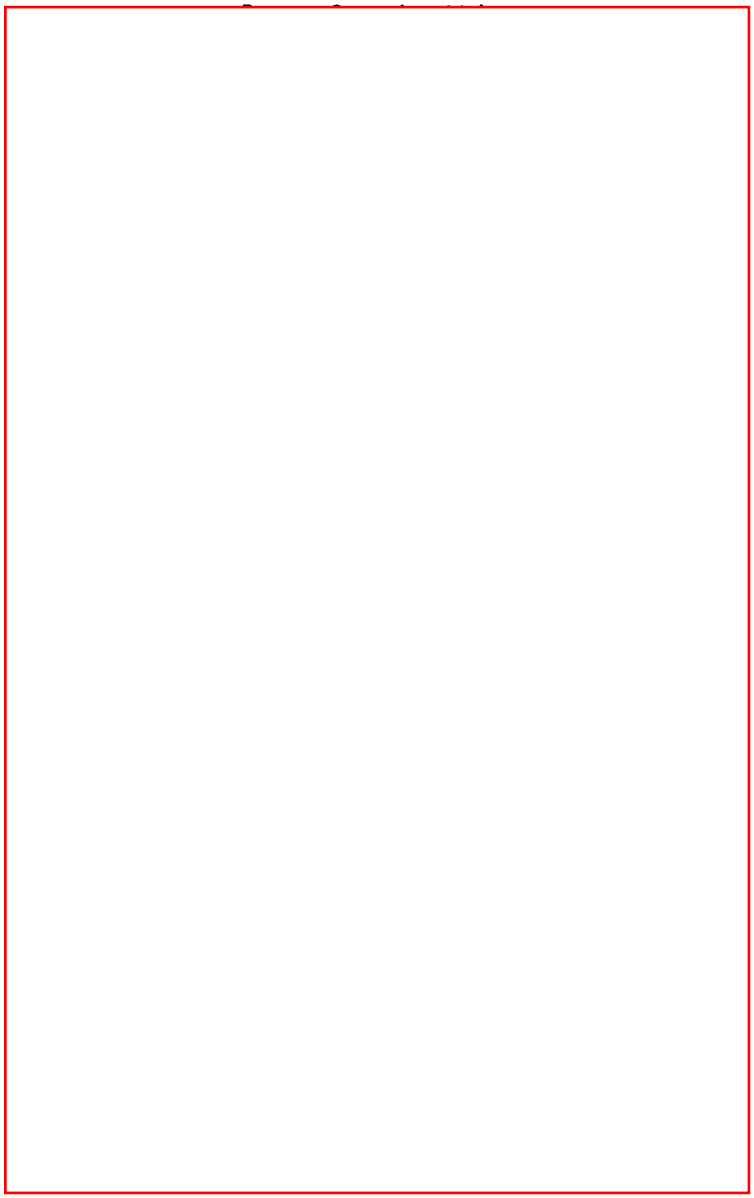


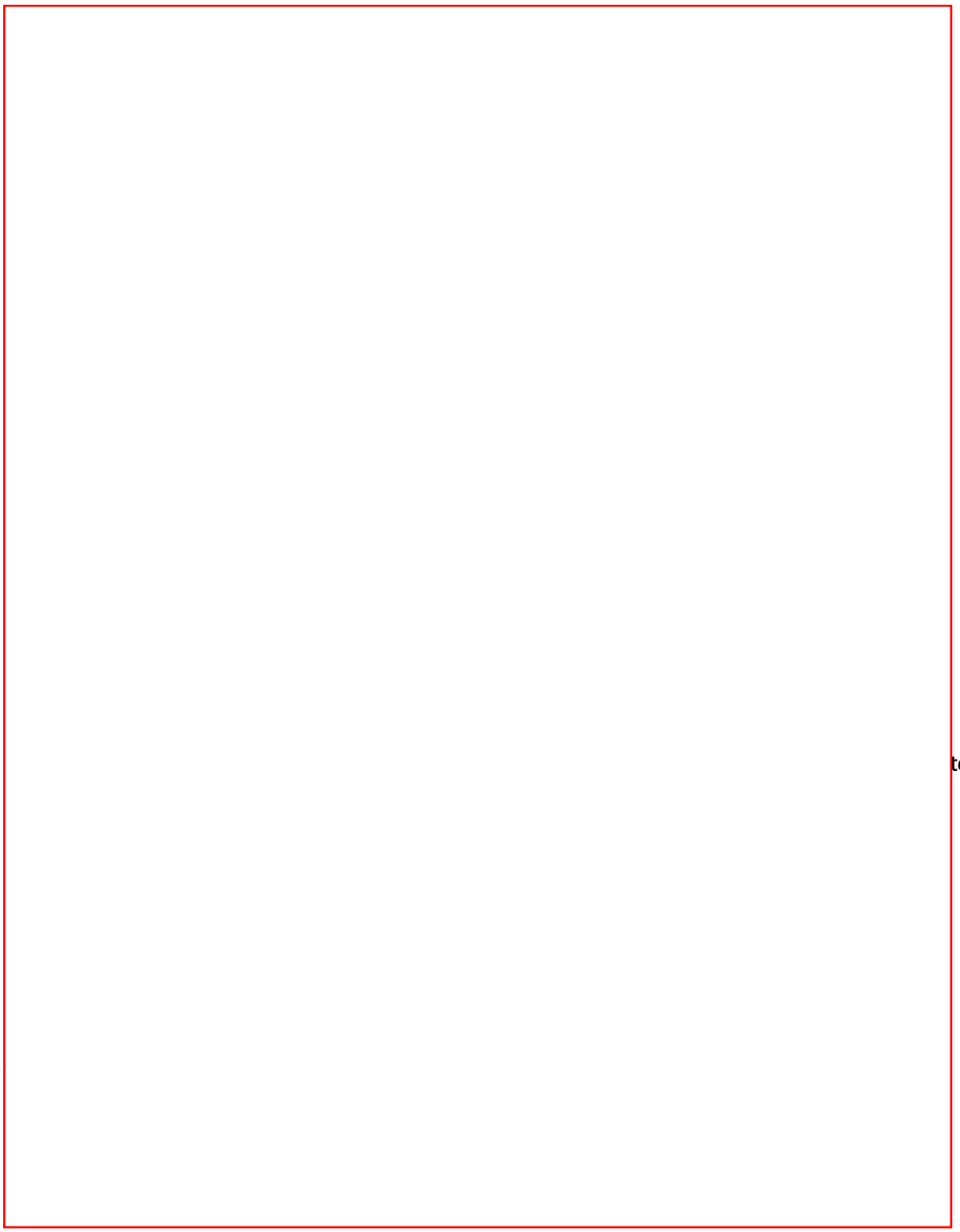
Table-2 (Currents measured in lab)

I_C	1.1986mA
I_E	1.2031mA
I_B	4.5μA

$$\beta = \frac{I_C}{I_B} = \frac{1.1986mA}{1.2031mA} = 262$$

$$\beta = \frac{I_C}{I_E - I_C} = \frac{1.1986mA}{1.2031mA - 1.1986mA} = 266$$





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f_H =

Appendix 5 – Circuit Diagrams

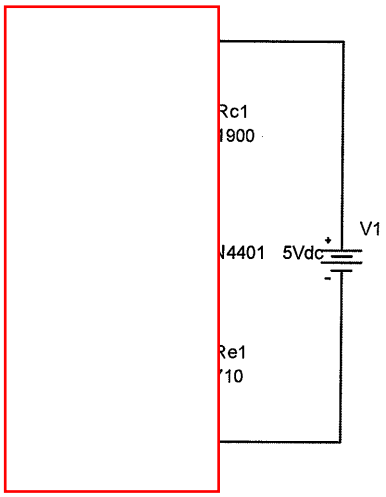

Figure -1 (DC portion of the single stage common emitter amplifier)

Figure-2 (Completed common emitter amplifier)