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EE 254
Project 6
12/6/13

Project 6: Oscillator Circuits

The purpose of this experiment was to design two oscillator circuits: a Wien-Bridge oscillator at 3 kHz oscillation and a Hartley Oscillator using a BJT at 5 kHz oscillation.

The first oscillator designed was a Wien-Bridge oscillator (Figure 1). Before designing the circuit, some background information was collected. An input signal sent to the non-inverting terminal with a parallel and series RC configuration as well as two resistors connected in inverting circuit types to achieve gain. The circuit works because the RC network is connected to the positive feedback part of the amplifier, and has a zero phase shift at a frequency. At the oscillation frequency, the voltages applied to both the inputs will be in phase, which causes the positive and negative feedback to cancel out. This causes the signal to oscillate.

To calc [redacted] as chosen [redacted] esistor to be 1 [redacted] 1.07Ω, the circ [redacted] ose to the calc [redacted]

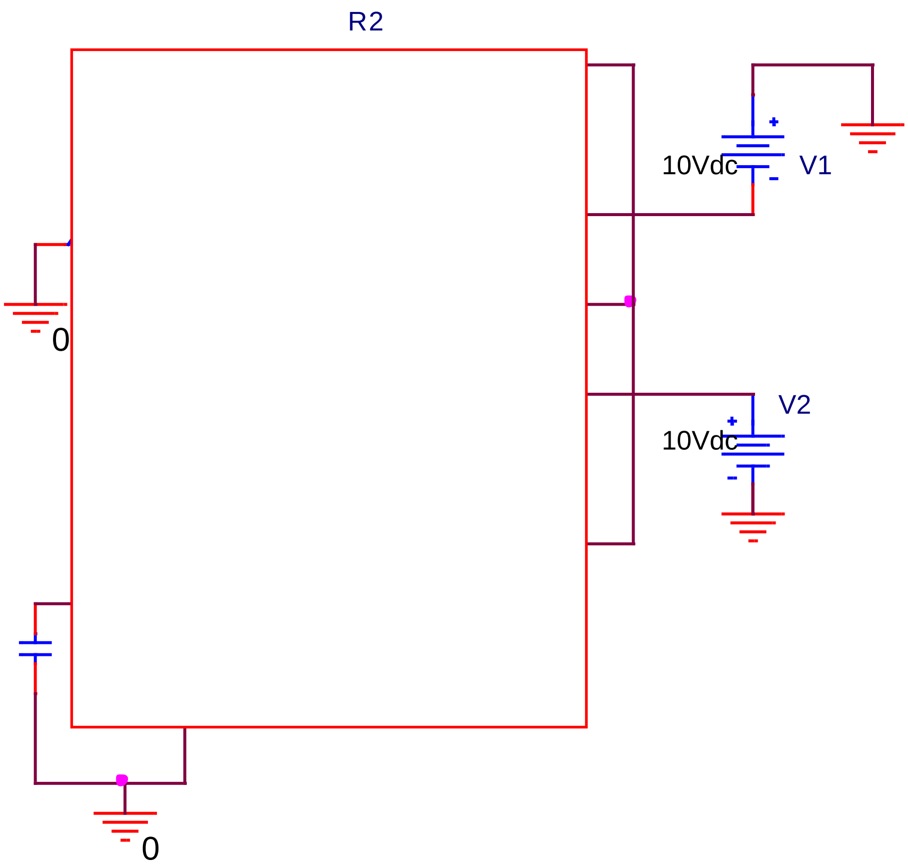

Figure 2: Wien-Bridge Oscillator built in PSPICE

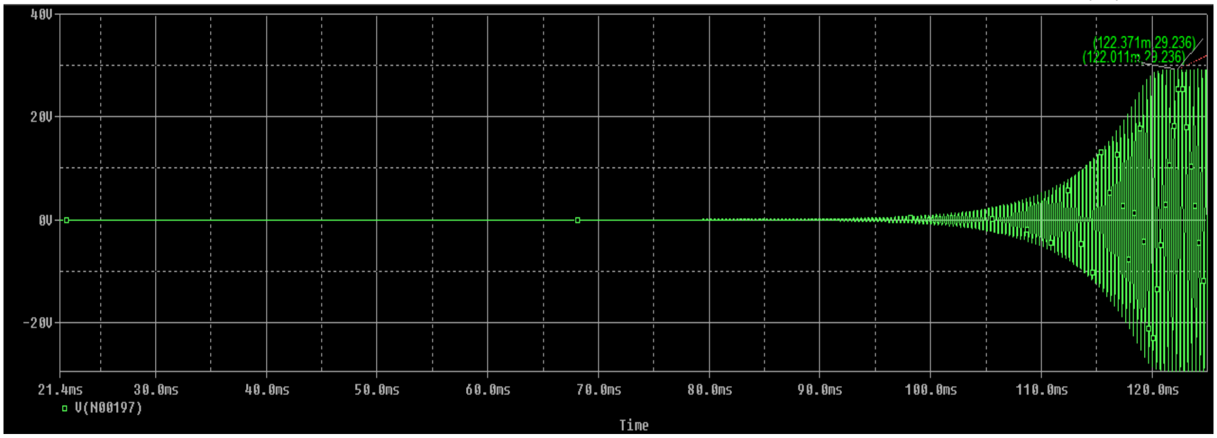

Figure 3: Simulation of circuit

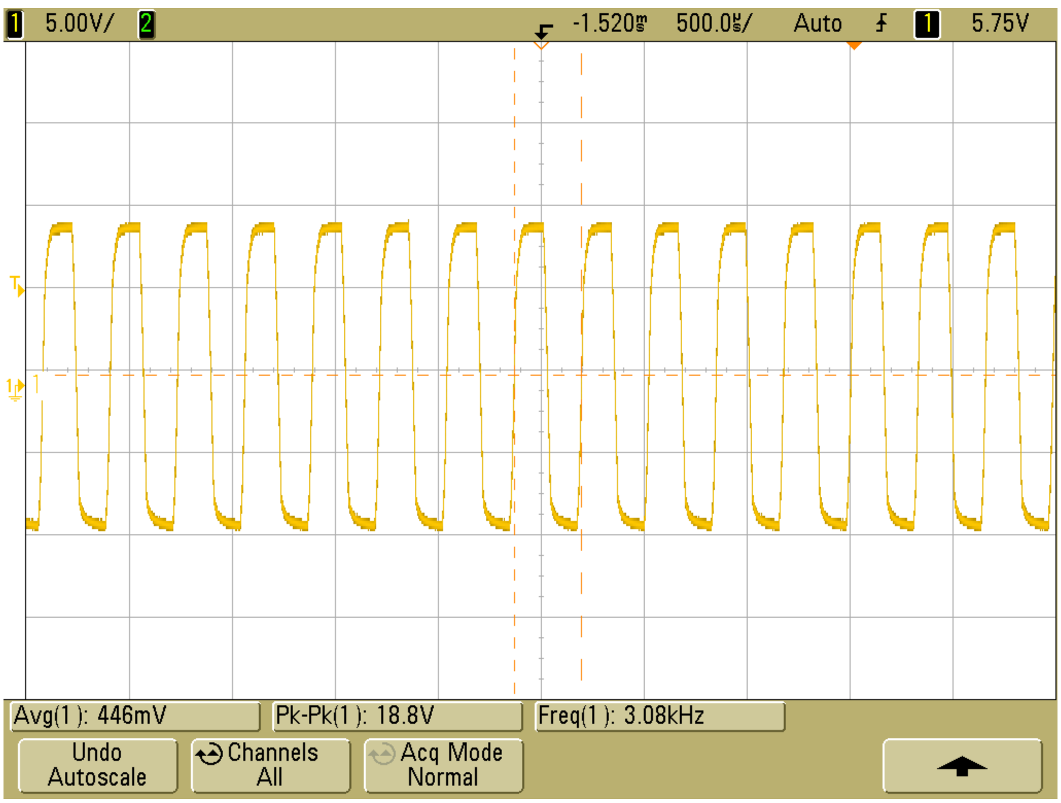

Figure 4: Oscillation of circuit at 3.08 kHz

The other oscillator was a Hartley BJT oscillator with an oscillating frequency of 5 kHz (Figure 5). It uses an LC circuit combined with a transistor for feedback. When the tank circuit (LC circuit) is working, the capac [redacted] th as the capac [redacted] oscillation, which [redacted] nt to be close to the [redacted] et the neces [redacted] ase shift in the feedb [redacted] rrents.

To ca [redacted] used. The capac [redacted] .02mH, and L2 was c [redacted] mulating, the time [redacted] conds to the calcul [redacted] approximately 5kHz, but probably a little higher.

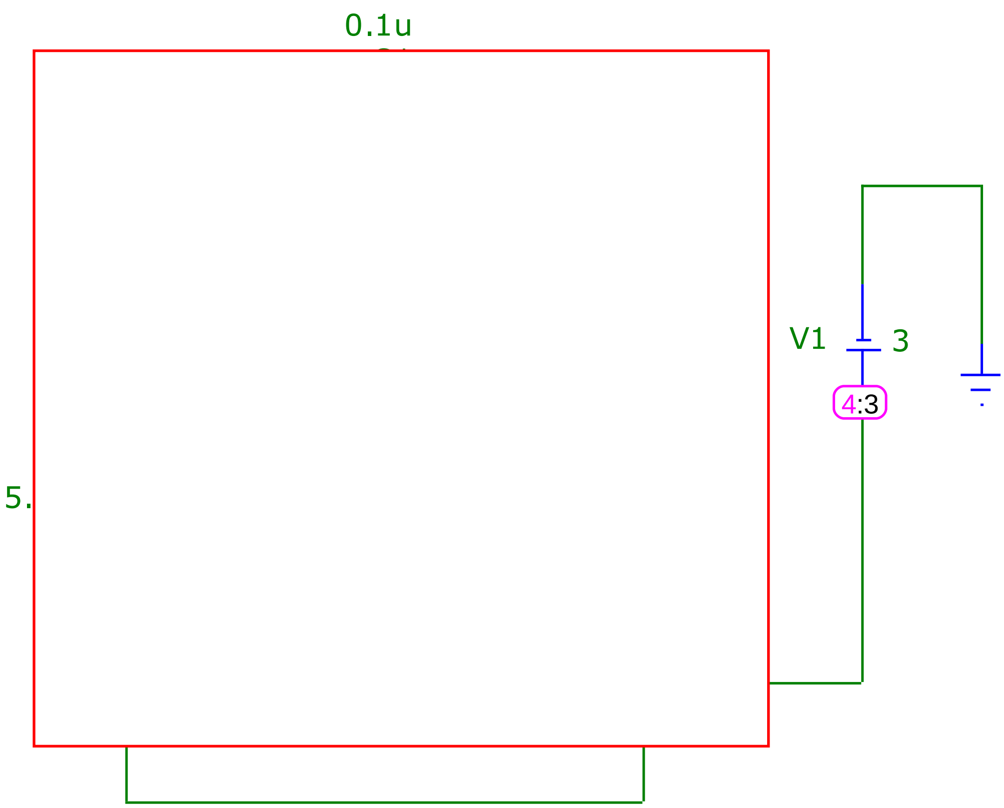

Figure 6: simulated Hartley oscillator circuit

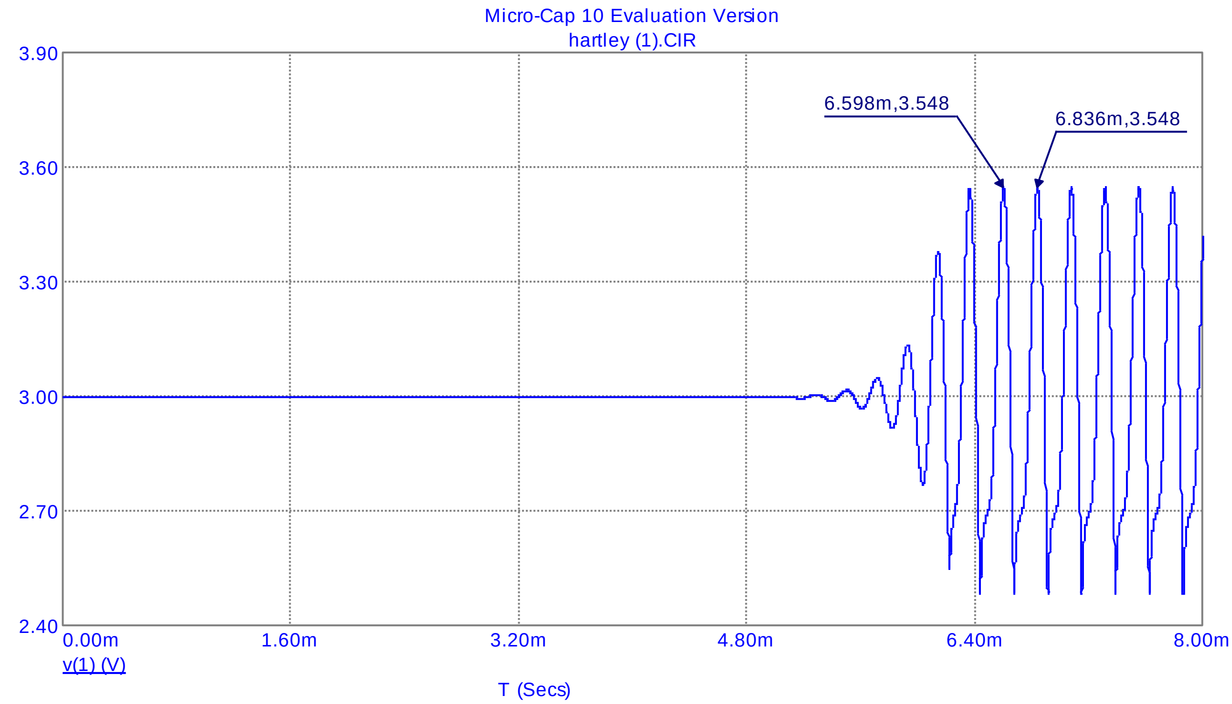

Figure 7: simulated output voltage with correct frequency

When b [redacted] esting the circuit, t [redacted] z instead of the 5.56 [redacted]

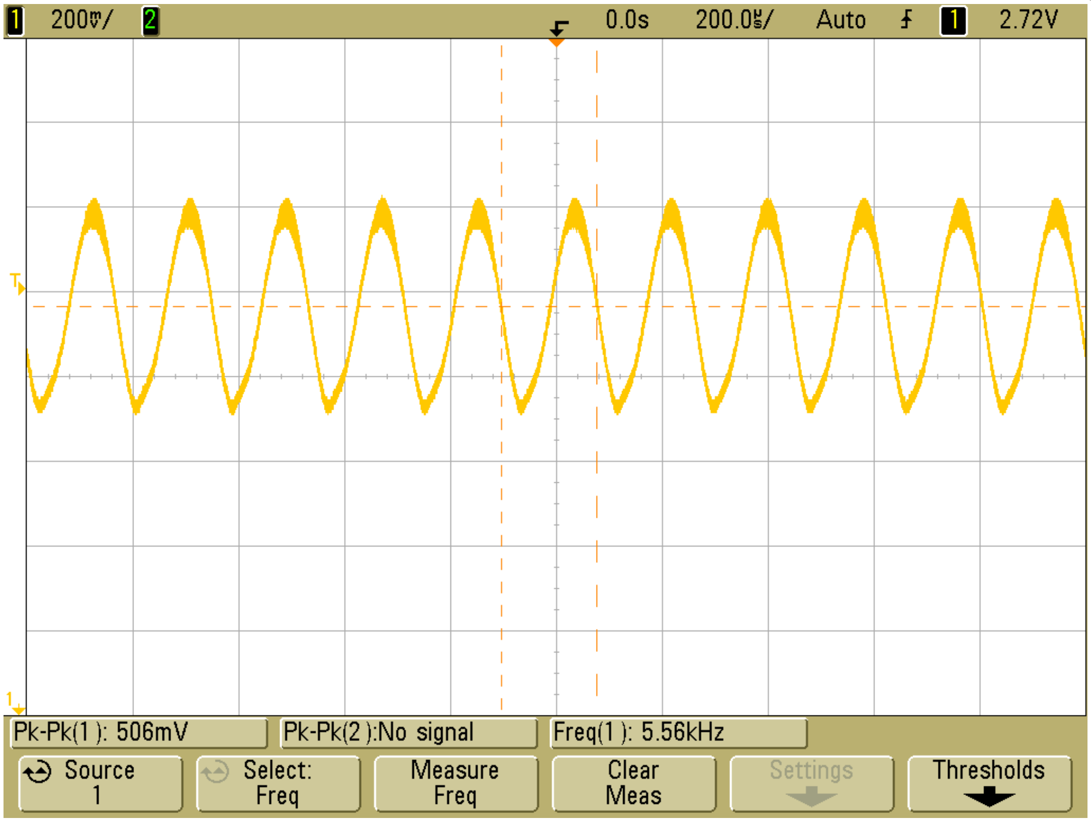

Figure 8: output voltage at 200 Ohms

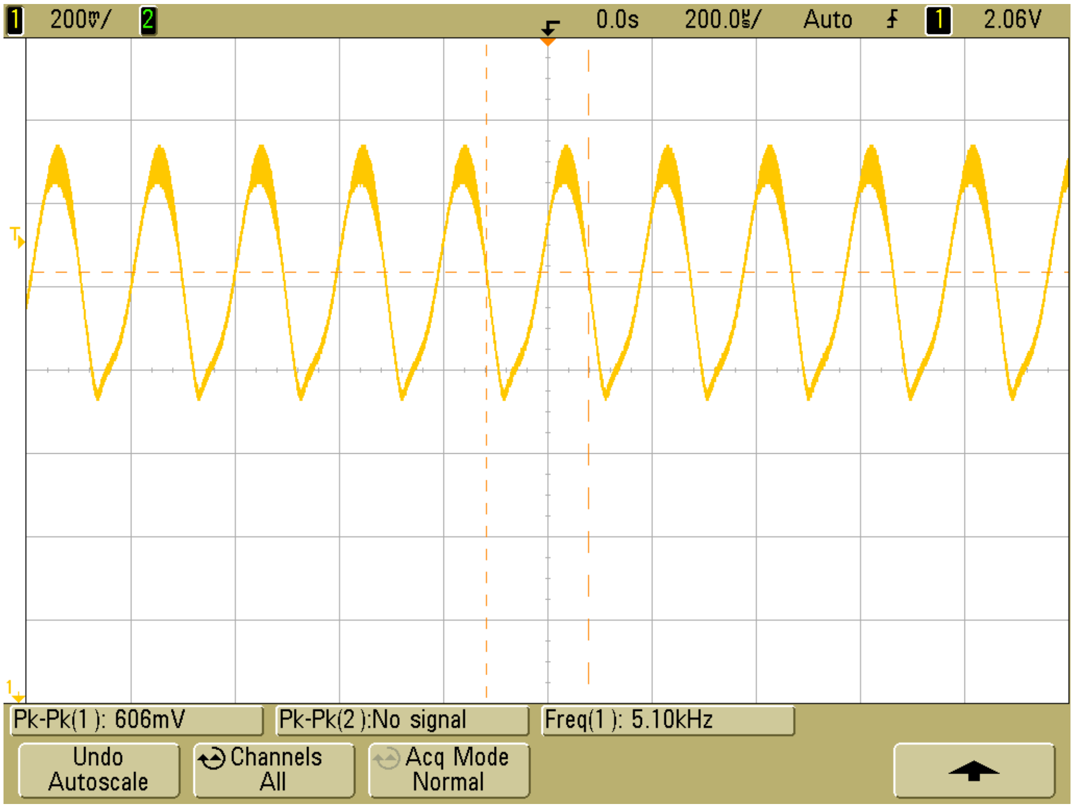

Figure 9: output voltage at 150 Ohms

Conclusion

After doing this experiment, the Wien Bridge oscillator was designed correctly, by using an RC network of parallel and series combinations in the non-inverting terminal of an op-amp, and positive feedback in the inverting terminal. The circuit worked as expected; by lowering the value of the resistor R2, the frequency was reduced to 3.08 kHz. The Hartley oscillator also worked; by using an LC circuit combined with positive feedback from a transistor with an emitter resistor for stability. The emitter resistor had to be lowered to get a value of 5.1 kHz, which was still higher than the design frequency of 5 kHz. The only other parameters that could be lowered would be the two inductors or the capacitor, which changes the design parameters.

[redacted]
EE 254
Project 6
12/6/13

[redacted] Circuit

[redacted] 30 Ω = R

[redacted] C using f

[redacted] 0333 s

[redacted] or f = 3000 Hz

$X_1 = 122.011$ ms
$X_2 = 122.346$ ms

$X_2 - X_1 = 0.000335$ s

Calculation 3: Actual time spacing from sim

[redacted]

EE 254

Project 6

12/6/13

C

[redacted]

...it

$f = \frac{1}{2\pi\sqrt{}}$ [redacted]

$5000 =$ [redacted]

Choos [redacted] 66mH

Calculation 4: Tank circuit Parameters

$f = 5kHz, \; T = \frac{1}{f} = \frac{1}{5000} = 0.0002s$

Calculation 5: Theoretical time Spacing

$X_1 = 6.598ms$ $\quad X_1 - X_2 = 0.000238ms$

$X_2 = 6.836ms$

Calculation 6: Actual time Spacing