Friday, March 15, 2013
11:48 AM

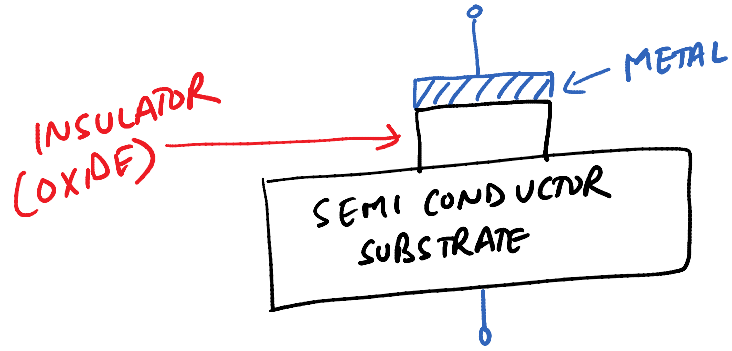
LECTURE - 36

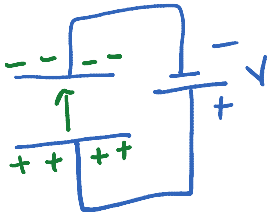
MOSFET

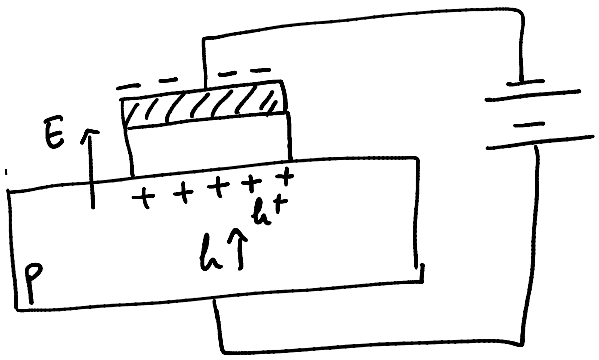
METAL OXIDE SEMICONDUCTOR FET

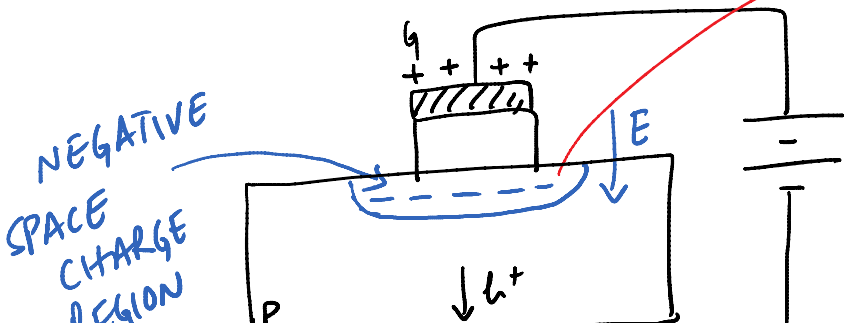
ADV. SMALL AREA → USED FOR DIGITAL CIRCUITS
VLSI IS POSSIBLE

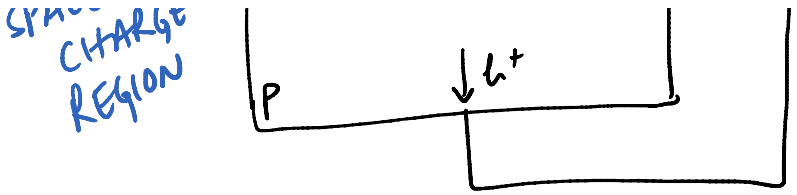
BASIC MOS CAPACITOR STRUCTURE

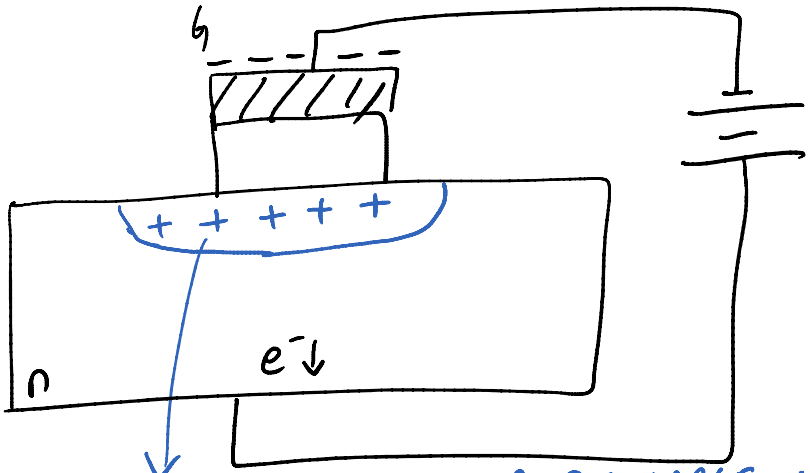












HOLE INVERSION LAYER FOR LARGE VOLTAGE

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ENHANCEMENT MODE → VOLTAGE MUST BE APPLIED TO THE GATE TO CREATE AN INVERSION LAYER

P-TYPE → POSITIVE GATE VOLTAGE

n-TYPE → NEGATIVE " "

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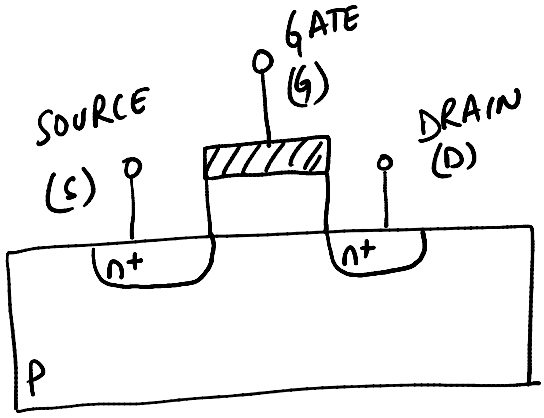
n MOS

n-CHANNEL ENHANCEMENT MODE MOSFET

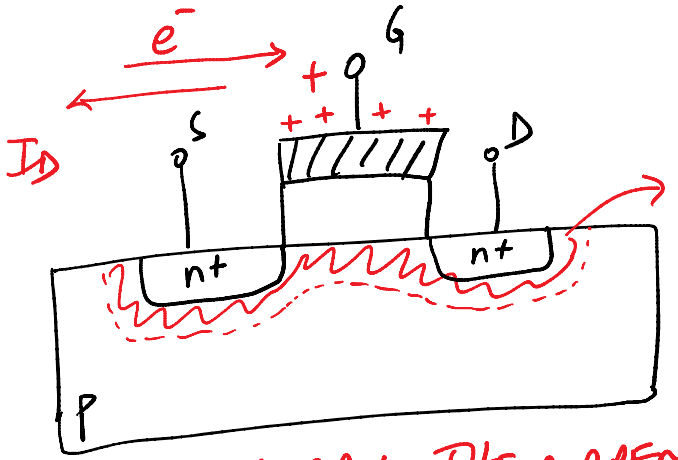
NORMALLY OFF DEVICE



* WITH NO BIAS, SOURCE AND DRAIN ARE ISOLATED BY P-REGION ∴ NO CONDUCTION

$I = 0$

IF A LARGE POSITIVE GATE VOLTAGE IS APPLIED AN ELECTRON INVERSION LAYER IS CREATED THAT CONNECTS n-SOURCE TO n-DRAIN → TO CAUSE ELECTRON FLOW



ELECTRONS CARRY THE CURRENT ∴ n-CHANNEL

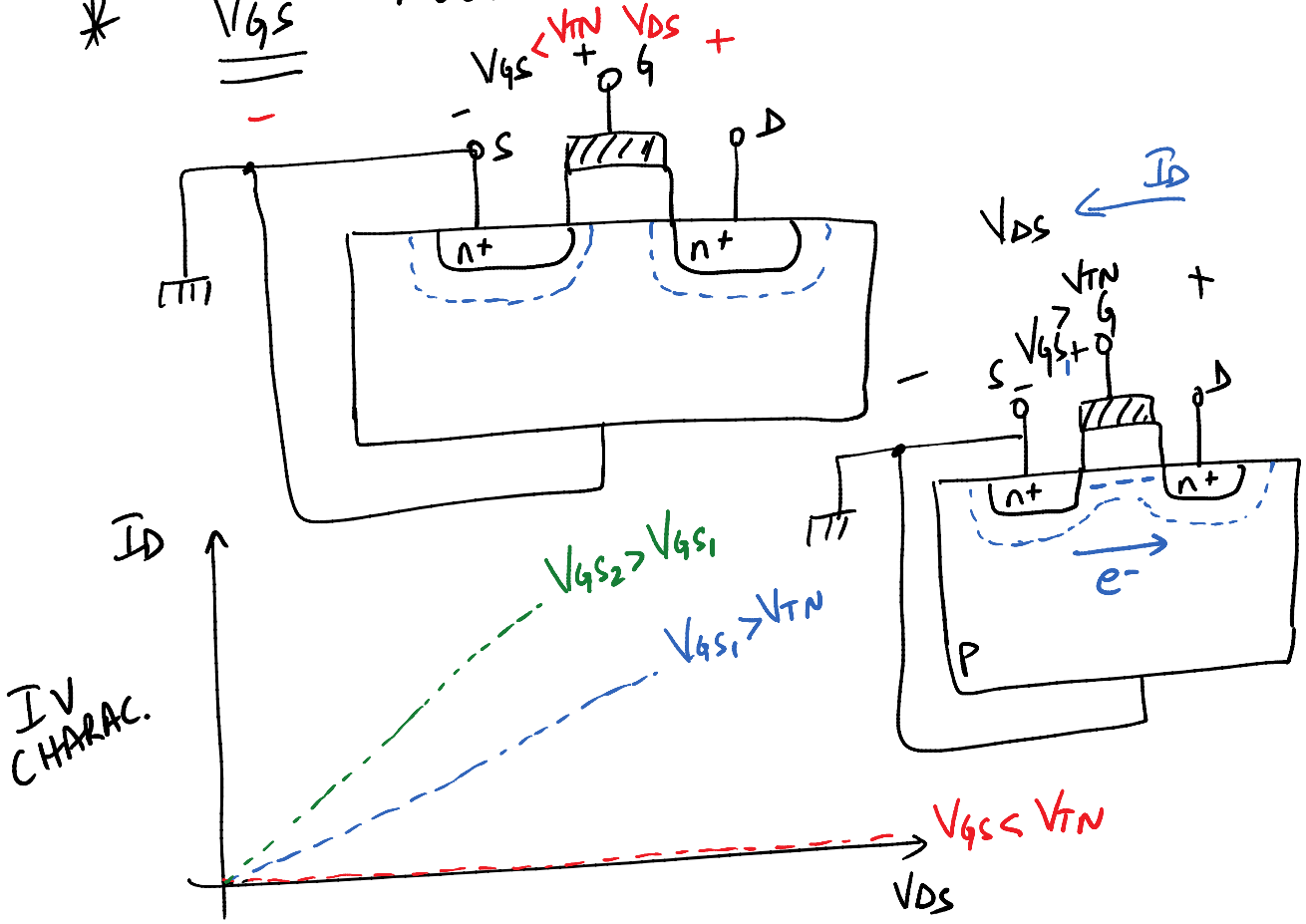
n-MOS

nMOS

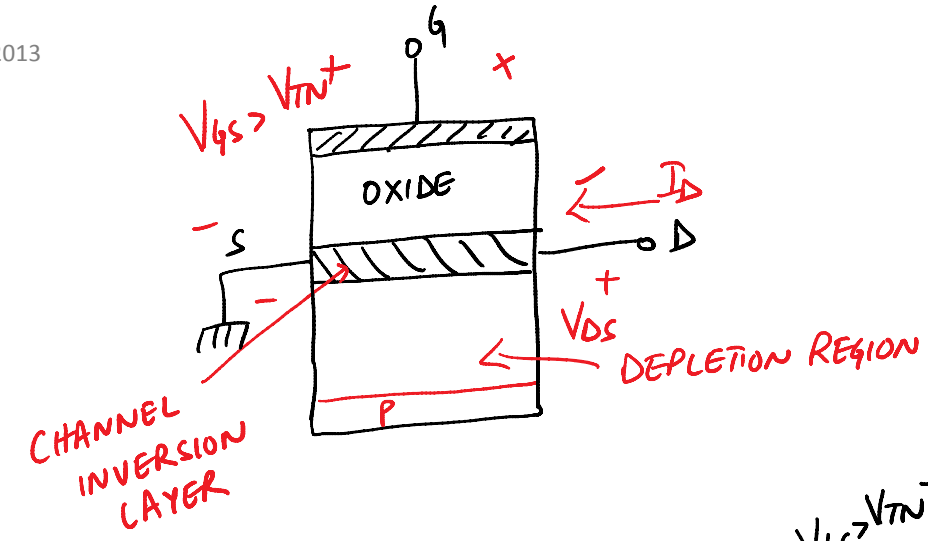
THRESHOLD VOLTAGE

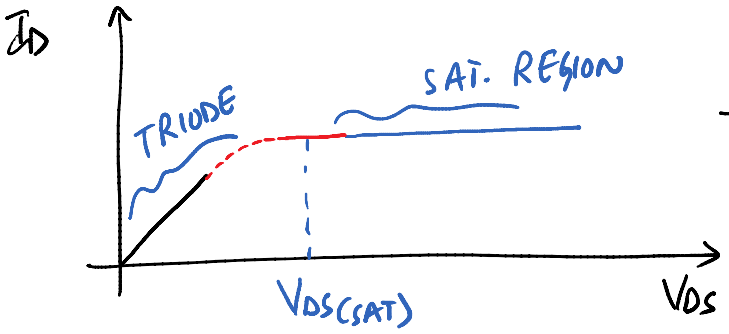
nMOS V_{TN}

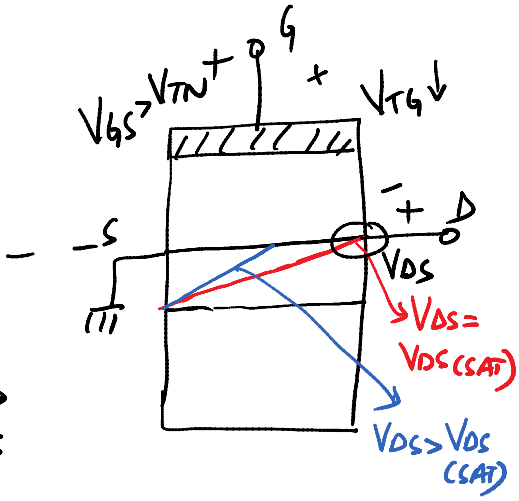
* V_{GS} NEEDED TO TURN-ON THE TRANSISTOR



IV CHARAC.







AS V_{DS} IS INCREASED TO ~~THE~~ THE POINT $V_{GS} - V_{DS} = V_{TN}$

INDUCED INVERSION CHARGE DENSITY IS ZERO NEAR THE DRAIN

$$V_{GS} - V_{DS(SAT)} = V_{TN}$$

OR

nMOS → $V_{DS(SAT)} = V_{GS} - V_{TN}$

$V_{TN} > 0$

ENHANCEMENT MODE

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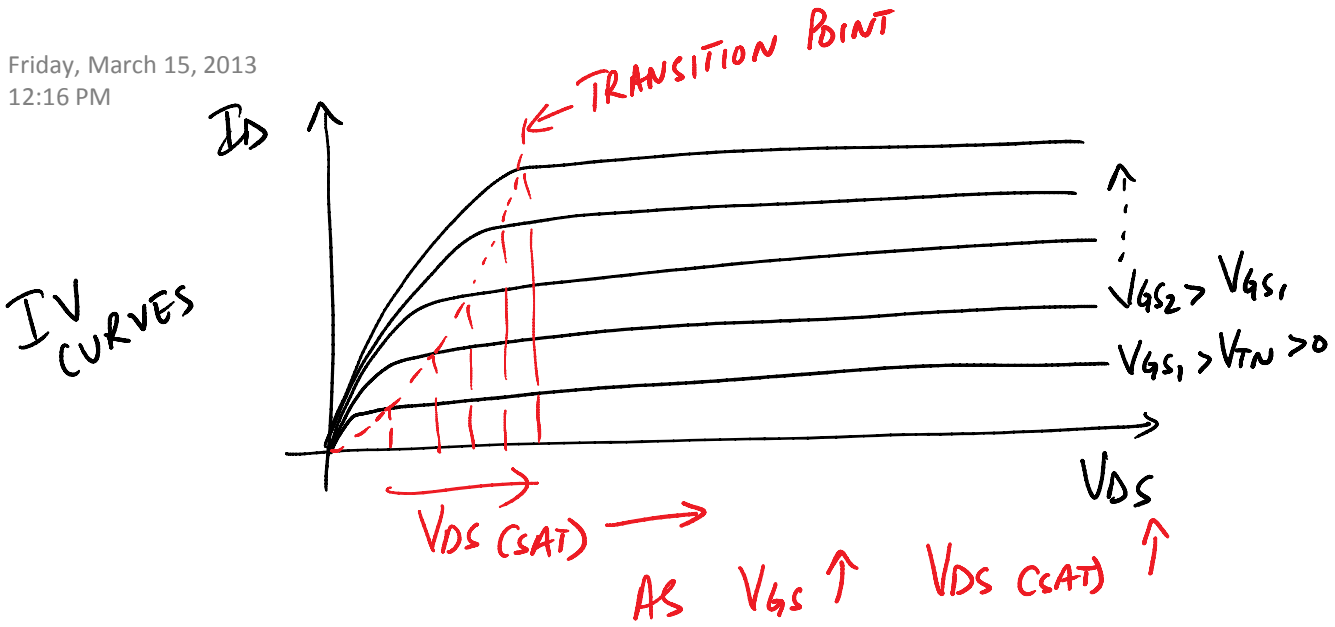

AS $V_{GS} \uparrow$ $V_{DS(SAT)} \uparrow$

nMOS

$V_{TN} > 0$

NON SATURATION / LINEAR ← TRIODE REGION

$$I_D = K_n \left[2 (V_{GS} - V_{TN}) V_{DS} - V_{DS}^2 \right]$$

SAT. REGION

$$I_D = K_n \left[V_{GS} - V_{TN} \right]^2$$

$V_{TN} > 0$

$K_n \rightarrow$ CONDUCTION PARAMETER

$I_D = I_{DS}$ $V_{DS(SAT)} = V_{GS} - V_{TN}$