TOTAL DOSE RADIATION EFFECTS FOR IMPLANTED BURIED OXIDES

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Abstract

The oxygen implantation process is now the most accepted means of forming an SOI substrate. We previously developed a technique, based on high frequency C-V measurements, for extracting the fixed charge, interface state, and doping densities at both of the interfaces associated with this buried oxide. Using this technique, we show for the first time the evolution of these charge densities with irradiation at both oxide interfaces. The densities of trapped holes (Q_{ot}) and generated interface states were found to be low. The effect of a substrate bias on the radiation response was characterized, showing that a bias exists that minimizes hole trapping, and that the substrate bias eliminates the differences due to the SIMOX process variations.

I. INTRODUCTION

Significant progress has been recently reported concerning the development of SOI integrated circuits for radiation-hardened applications [1-10]. The SIMOX process [11], or oxygen implantation, has emerged as the leading SOI technology for these applications. It is important to note that these applications are largely radiation hardened, so that the radiation response characteristics of the buried oxide formed by the SIMOX process are of significant interest. Furthermore, since the process of forming SIMOX buried oxides is quite different from the growth of conventional thermal gate oxides, the radiation response of this oxide is of significant scientific interest.

Work to date concerning the radiation response of the buried oxide has centered on controlling the back-channel leakage in the NMOS transistor. Several groups [1,5,6] have established that a negative substrate voltage is very useful in controlling the transistor characteristic under total dose, and that a substrate voltage exists at which the back-channel threshold shift under total dose is minimized. Some information concerning the interface state characteristics of this interface has also been extracted. These works include analysis of threshold shifts [5,6,12], electron spin resonance (ESR) studies [13], and a technique based on a deconvolution of the SOI structure by etch-back [14]. However, very little work has been done to thoroughly characterize the various components of radiation induced charges in this oxide. In this paper, we present a characterization of the interface states, fixed oxide charge and trapped holes at both interfaces of the buried oxide layer, as radiation dose, substrate bias and processing are varied. This characterization is based on analysis of high frequency C-V curves of the buried oxide layer. Since there are two Si/SiO_2 interfaces in this system, conventional MOS capacitor analysis cannot be used. Instead, a theoretical C-V relation is fitted to the experimental C-V curve, and the various charges obtained from the best fit. The details of this theory have been published elsewhere [15]. Additionally, the results are correlated with an analysis of the N- and P-channel backgate transistor response.

II. EXPERIMENTAL DETAILS

N-type, 3-5 ohm-cm silicon wafers received oxygen implants, using the NV-200 (100 mA class) oxygen implanter. The wafers were implanted to a dose of $1.8 \times 10^{18} cm^{-2}$, and were heated to 500-550 C during the implant by beam heating. Following the oxygen implant, the wafers were annealed at either 1250 or 1285 C for 2 to 16 hours, in an N_2/O_2 ambient. Test devices were then fabricated.

Samples were irradiated with 10 keV X-rays using the Aracor 4100 Semiconductor Irradiation System. Total dose was varied from 10 krad(SiO_2) to 1 Mrad(SiO_2). During irradiation, devices were biased in the following manner: the sources, drains, and body contacts of the N-and P-channel backgate transistors were tied together and grounded, as was the silicon film electrode for the N- buried oxide capacitor. The top gate of the P-channel transistor was given a -5V bias, and the top gate of the N-channel transistor given a 5V bias. The substrate bias (V_{sub}) was varied between -5

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and +5 volts, depending on the desired conditions. The purpose of this bias arrangement is to insure that the applied electric field across the buried oxide was identical for the capacitors and backgate transistors. N- and P-channel threshold voltage and subthreshold slope measurements were performed immediately following irradiation, using an HP 4145 Semiconductor Parameter Analyzer. Following transistor measurements, C-V measurements were performed using an HP 4175 LCR meter. To simplify the C-V analysis, trapped charge is modeled as a sheet of charge at each interface, neglecting the distribution of holes into the oxide bulk. The X-ray dosage was not normalized to Cobalt-60 dosage, nor were dose enhancement effects taken into account [16].

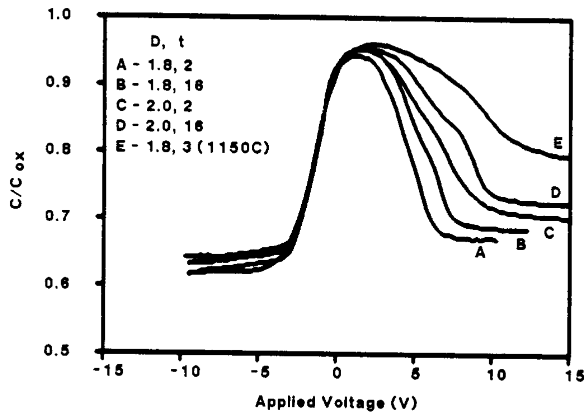

Figure 1: Example of high frequency C-V curves for various buried oxide capacitors preirradiation. C_{ox} refers to the oxide capacitance, while the applied voltage refers to the bias applied to the film with the substrate grounded. The units of D and t are $10^{18}cm^{-2}$ and hours, respectively. Devices A through D were annealed at 1250°C.

The effects of implant dose and anneal time on unirradiated samples are shown in Figure 1 to illustrate the C-V analysis technique. Note that since both the film and substrate are n-type, when the substrate is grounded, a positive bias depletes the film/oxide interface while a negative bias depletes the substrate/oxide interface. In this figure, it is seen that the positive bias region of the C-V curve is affected by the process changes, while the negative bias region is not. This indicates that nearly all of the effects of these processes occur at the upper (device layer) interface. Since interface traps stretch out C-V curves while fixed oxide charge causes a rigid shift, it is seen that the increase of anneal time increases the fixed charge density without increasing the surface states, but the increased implant dose increases both parameters [15].

III. EXPERIMENTAL RESULTS

The main results of this study are shown in Figures 2 through 7. Note that in these figures and in the following discussion, all voltage shifts stated are absolute values, unless otherwise noted. The uncertainty is approximately the size of the points. In Figure 2, the effect of increasing the X-ray dose on the back-channel transistors and on the buried oxide capacitor is shown, for the case of a grounded substrate. The midgap voltage, V_{mid}, is defined as the voltage shift for which the Fermi level at the Si/SiO_2 interface is in the middle of the bandgap. Although both donor and acceptor

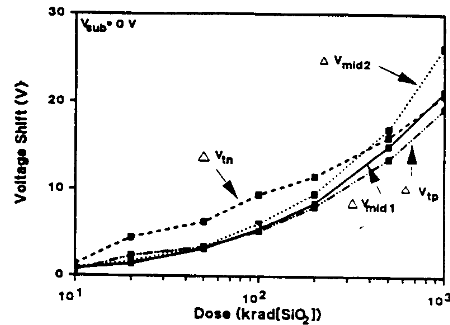

Figure 2: Magnitude fo voltage shift versus x-ray dose for the buried oxide capacitor and for n- and p-channel back interface transistors, for the case of the substrate grounded during irradiation. The threshold voltage shifts for the n- and p-channel transistors are denoted as $\Delta V_{tn,tp}$ while $\Delta V_{mid1,mid2}$ denote the midgap voltage shift at the film/oxide and substrate/oxide interfaces, respectively.

type traps are found in both halves of the bandgap [17,18], the neutral point is only a few kT/q from midgap [18] (for ionizing radiation). Thus, V_{mid} is a good approximation of the voltage shift due solely to oxide charge. The threshold voltage for MOSFETs (V_t), on the other hand, is related to the sum of oxide charge and interface traps at the energy level corresponding to the onset of inversion. Since a good correlation is seen between V_{mid} and V_t, few interface traps are being created. The effect of a negative substrate bias during irradiation can be seen in Figure 3. A negative bias reduces the trapping of holes, especially above 100 krad. The curves for V_{mid1} and $V_{tn,p}$ are essentially parallel, showing that very few interface states are generated, even at 1Mrad. This result can be seen more specifically in Figure 4, in which the subthreshold slope and interface state density are both plotted versus dose. Even at a dose of 1 Mrad, the subthreshold slopes are close to their pre-irradiation values and the density of midgap interface states that have been created is only $1x10^{11}eV^{-1}cm^{-2}$.

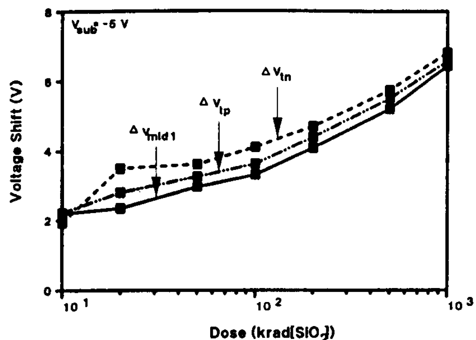

Figure 3: Magnitude of voltage shift versus x-ray dose for the buried oxide capacitor and for n- and p-channel back interface transistors, for the case of -5 V bias on the substrate during irradiation. The threshold voltage shifts for the n- and p-channel transistors are denoted as $\Delta V_{tn,tp}$ while $\Delta V_{mid1,mid2}$ denote the midgap voltage shift at the film/oxide interface.

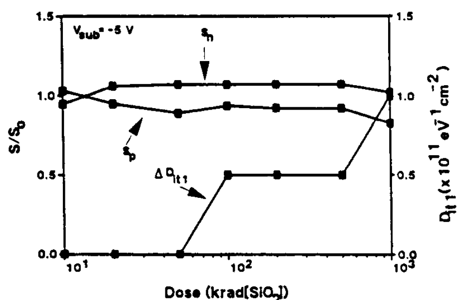

Figure 4: Degradation of the subthreshold slope for the n- and p-channel back-gate transistors and generation of midgap interface traps as a function of dose. The quantities S_n and S_p represent changes in the subthreshold slopes of the n- and p-channel devices, while D_{it1} represents the density of interface traps generated at the film/oxide interface. A substrate bias of -5 V was applied during irradiation.

The effects of a -5V bias relative to zero volts during irradiation can be seen even more clearly in Figure 5. This figure shows the density of trapped charge for both interfaces as a function of dose for substrate biases of 0 and -5 volts. Note that roughly equal densities of charge are trapped at both interfaces for a 0V bias, while the -5V bias greatly enhances the trapping of holes at the substrate/oxide (S/O) interface, even at a dose of only 10 krad. The film/oxide (F/O) trapped charge density is reduced by the -5 volt bias, and the response is approximately linear with dose. Previous work on the total dose response of buried oxide layers has indicated that there is a bias region for which the trapping of charge is minimized. In order to investigate this effect, we plotted V_{mid1} as well as $V_{tn,p}$ as a function of substrate bias in Figure 6.

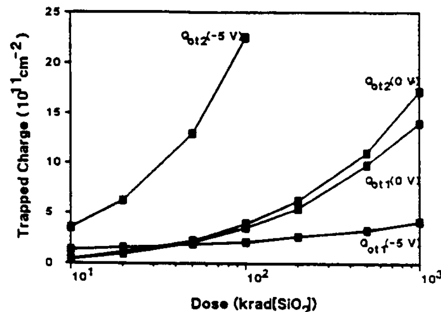

Figure 5: Comparison of trapped charge at both buried oxide interfaces for the cases of 0 and -5 V substrate biases during irradiation. The subscripts "1" and "2" refer to the film/oxide and substrate/oxide interfaces, respectively.

The plot is for a dose of 100 krad. It is seen that V_{tn} is minimized by a -3V bias, V_{tp} by a -2V bias, and that V_{mid1} is essentially unchanged from -2 to -4 volts. The minimum exists due to three competing effects, which may balance differently in the three cases cited [19]. The first effect is that an increase of electric field means that a higher percentage of generated electron-hole pairs escape geminate recombination. Thus, more holes survive to be trapped at an interface.

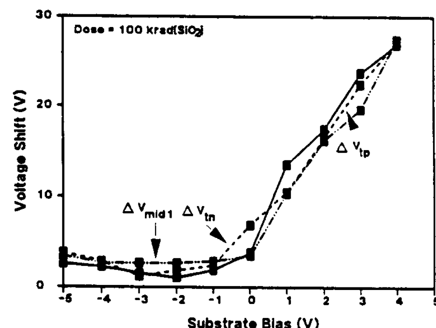

Figure 6: Effect of substrate bias on the magnitude of the film/oxide midgap and back-gate voltage shifts for a dose of 100 krad (SiO_2).

The second effect is that as an increasingly negative bias is applied to the substrate, holes are driven away from the F/O interface. The third effect is that the capture cross section is inversely related to the electric field. The sum of these effects is that an electric field exists that minimizes charge trapping at a given interface.

IV. DISCUSSION

The pre-irradiation density of electrically-active defects is much higher in the film and at the F/O interface than in the substrate and at the S/O interface [15,20]. To see how this affects the post-radiation charge trapping characteristics, we plot both Q_{ot1} and Q_{ot2} versus substrate bias in Figure 7. For a bias of 0V or one that attracts holes to the interface, the F/O interface traps slightly fewer holes than does the S/O interface. It is interesting that although $Q_{f1} > Q_{f2}$, $Q_{ot1} < Q_{ot2}$. For an attractive bias, the rate of charge buildup is $3.8 \times 10^{11} cm^{-2}V^{-1}$ at the F/O interface and $3.9 \times 10^{11} cm^{-2}V^{-1}$ for the S/O interface. This implies that despite the higher density of fixed charge and interface traps at the F/O interface pre-rad, the number of

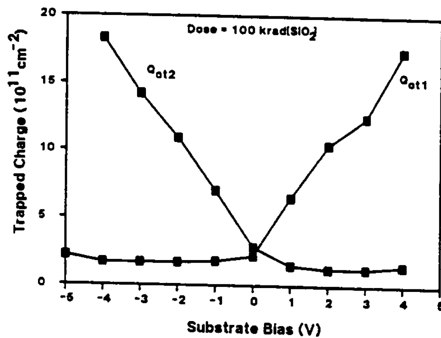

Figure 7: Effect of substrate bias on trapping of charge at the film/oxide and substrate/oxide interfaces, for a dose of 100 krad (SiO_2). The quantities Q_{ot1} and Q_{ot2} refer to the film/oxide and substrate/oxide interfaces, respectively.

radiation-induced hole traps is nearly the same at both interfaces. However, when holes are being driven away from the interface under consideration, the S/O interface traps less holes, as seen by the fact that the minimum Q_{ot} is lower for the S/O interface than for the F/O interface. Since silicon islands are found in the buried oxide layer near the S/O interface, but not near the F/O interface, it might be expected that the S/O interface would have more traps than the F/O interface. That the minimum Q_{ot} is lower for the S/O interface than for the F/O interface may be related to the lower pre-rad Q_f at this interface. The local internal electric field may also play a part. In Table 1, we compare the charge trapping properties of two SIMOX samples processed somewhat differently. As can be seen, for V_{sub} = 0V, sample 419 traps more holes at both oxide interfaces than does sample 1311, while a -5V bias essentially eliminates this difference. The thickness of the buried oxide layer is identical for the two samples. However, pre-irradiation analysis of the samples showed that sample 1311 had significantly fewer defects than sample 419, especially metallic contaminants [21]. Metal contaminants in the buried oxide layer may increase carrier trapping by acting as carrier traps, or by forming bonds that are easily broken. Overall, the comparison of the two samples implies that zero-bias charge trapping is reduced in higher quality SIMOX wafers. Interestingly, a -5V substrate bias equalizes the radiation response of 1311 and 419. This shows that even a small electric field (about 1×10^5V/cm) has a major impact on carrier transport in the oxide.

Clearly, the total-dose hardness of buried oxide layers is greatly improved by the use of a negative substrate bias during irradiation. The threshold voltage shifts presented here are typical of our experience with SIMOX buried oxides. Since the voltage shifts for a zero volt substrate bias are significant, a negative bias is used during radiation at high total doses to reduce the amount of trapped holes and thereby keep the circuits functional. Technically, the negative substrate bias is beneficial. However, from a systems designer perspective, the need for an additional supply and/or pin compatibility can be major issues, and a circuit requiring a negative substrate bias may not be acceptable.

SUMMARY

An evaluation technique for studying the charge buildup over total X-ray dose by high frequency C-V analysis has been presented. It has been shown that the technique is useful for evaluating the various process, bias, and dose effects on the fixed charge and

Table I. Comparison of the charge trapping properties for two SIMOX processes. Devices were irradiated with 10 keV x-rays to a total dose of 100 kRad[SiO_2]. Substrate bias was 0 or -5 V. Shown is the change in oxide charge at the film/buried oxide interface (Q_{ot1}) and at the substrate oxide interface (Q_{ot2}).

	V_{sub} = 0 V		V_{sub} = -5 V	
Process	Q_{ot1} (10^{11} cm^{-2})	Q_{ot2} (10^{11} cm^{-2})	Q_{ot1} (10^{11} cm^{-2})	Q_{ot2} (10^{11} cm^{-2})
419	3.5	3.9	2.1	22
1311	2.2	2.9	2.2	22

interface state densities at the silicon/buried oxide interface. The buried oxide layers were found to have a low rate of trapped hole buildup, and a very low rate of interface state generation. A negative bias was found to reduce the buildup of charge at the film/oxide interface, and a bias region was found for which charge trapping was minimized. A comparison of the radiation response of the two buried oxide interfaces revealed that for a 0V substrate bias, or one that attracts holes to the interface, the film/oxide interface has less charge buildup, while a bias that drives holes away from the interface, the substrate/oxide interface has less charge buildup. Finally, in a comparison of the two SIMOX samples with different processing, the sample that had fewer pre-radiation defects was found to have less charge trapping at a 0V substrate bias, but to have the same charge trapping at a -5V substrate bias.

Acknowledgement

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