The Effects of Substrate Doping Density on The Electrical Performance of Through-Silicon-Via (TSV)

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Abstract — In this paper, the existing lumped circuit model for Through-Silicon-Via (TSV) structure embedded in Lightly-doped silicon substrate is reviewed and improved. A new lumped circuit model for TSV structure in heavily-doped silicon substrate is proposed. The underlying physics associated with the proposed lumped elements in the circuit topology is discussed and their values are found by data fitting using 3D full-wave simulation results. To the best of the authors’ knowledge, this is the first in-depth study on TSV modeling with consideration of different substrate doping densities. The proposed circuit model will be useful for signal integrity and power integrity design in 3D IC structures.

Keywords - Through-Silicon-Via (TSV); substrate doping density; lumped circuit model; electrical performance

I. INTRODUCTION

System-in-Package (SiP) technology is widely used today in high-density and small mobile devices such as smart phones, digital cameras, media players, and so on. Three-dimensional (3D) IC technology is being considered as a real breakthrough that can be used to more effectively achieve high density and high performance with vertically stacked heterogeneous ICs. Through-Silicon-Via (TSV) is the most promising interconnect design in 3D ICs which routes the electrical path through all stacked chips. TSV shortens the connection between vertical stacking chips which leads to better electrical performance and more compact size of the system [1]-[4]. A typical TSV structure can be found in Figure 1.

Since TSV is embedded in a silicon substrate, which has quite different material properties compared to a dielectric substrate, and there is a silicon-dioxide insulator layer between the metal via and the silicon substrate, the TSV structure is quite different from the conventional printed circuit board (PCB) via structure. Depending on the application, the substrate can be heavily-doped (e.g., $\sigma = 10k$-100 kS/m) for digital applications in order to guarantee that the entire substrate is equal-potential to reduce the possibility of latch-ups; it can also be lightly doped for analog circuits (e.g. $\sigma = 10$ S/m) to provide better isolation between components. In view of this, we argue that it is necessary to specially investigate the impact of substrate in the TSV modeling for signal integrity and power integrity. The TSV structure inside a lightly-doped silicon substrate has been investigated and a lumped circuit has been proposed in [4]. In our study, we find that the doping density of the silicon substrate will change the field distribution significantly in the TSV structure. As a result, the lumped circuit model developed for the lightly-doped case is no longer valid any more for the heavily-doped silicon substrate case. In this paper, we will improve the lumped circuit model developed for the TSV in lightly-doped silicon substrate and propose a new circuit model for the TSV in heavily-doped silicon substrate.

II. MODELING OF TSV IN LIGHTLY-DOPED SILICON SUBSTRATE

We start with the lightly-doped substrate with a conductivity of 10 S/m. This is a typical value for analog/RF applications. The structure of a pair of signal and ground TSVs is shown in Figure 2. [4].

The center-to-center distance of the two TSVs is denoted as $T_P$ which is 20 $\mu$m in our example; the TSV length is denoted
as \( T_L \) which is 20 \( \mu \text{m} \); the TSV diameter is denoted as \( T_D \) which is 10 \( \mu \text{m} \); the thickness of \( \text{SiO}_2 \) is denoted as \( T_T \) which is 0.2 \( \mu \text{m} \). The permittivity of the insulator is 3.9 and the permittivity of the silicon substrate is 11.9.

This structure was modeled with a 3D full-wave simulator (Ansys HFSS), and the E-field distribution was obtained as shown in Figure 3. The excitations of 1V and -1V were applied across the two TSV conductors on the top and bottom surfaces, respectively.

![E-field distribution for TSVs in a lightly-doped silicon](image)

The lumped circuit model proposed in [4], as shown in Figure 4, was adopted for this example with improved formulas developed for element calculations. Here the lightly-doped silicon substrate was treated as a lossy dielectric material so that the shunt path between two TSVs can be modeled using the circuit components in Figure 4. Since the \( \text{SiO}_2 \) insulator layer is very thin, the capacitance \( C_1 \) between the TSV and the silicon substrate can be approximately obtained from the coaxial capacitance formula although the lightly-doped silicon substrate is not a good conductor. Meanwhile, the silicon substrate between the two TSVs can be modeled as a shunt conductance \( G_0 \) (due to the conductive loss of silicon) in parallel to \( C_2 \) (due to the displacement current between the two TSVs through the silicon substrate). Therefore \( C_1 \), \( C_2 \) and \( G_0 \) can be approximately calculated using the following formulas:

\[
C_1 = \frac{2\pi \varepsilon_{\text{SiO}_2} T_L}{\ln \left( \frac{T_D + 2T_T}{T_D} \right)} \quad (1)
\]

\[
C_2 = \frac{\varepsilon_0 \pi T_L}{\ln \left( \frac{T_D T_T}{T_D + \left( T_T T_D / T_D \right)^2 - 1} \right)} \quad (2)
\]

\[
G_0 = \frac{\sigma_0 C_2}{\varepsilon_{\text{Si}}} \quad (3)
\]

A 2D cross-sectional analysis (Ansys Q2D) was also performed for this TSV structure and the per-unit-length RLGC parameters were obtained and normalized to the TSV length. The C and G values calculated by the 2D cross-sectional analysis were then used to fit the \( C_1 \), \( C_2 \) and \( G_0 \) values. The results were 103 fF, 5.06 fF and 0.5 mS, respectively. The calculated values of \( C_1 \), \( C_2 \) and \( G_0 \) for our example using (1) ~ (3) were 111 fF, 5.03 fF and 0.5 mS, respectively, which are quite similar to the fitted values from the 2D cross-sectional results.

Due to the skin effect, both \( R_T \) and \( L_T \) in Figure 4 change with frequency. \( R_T \) is proportional to the square root of frequency while \( L_T \) is proportional to the inverse square root of frequency at high frequencies. Then, \( R_T \) and \( L_T \) can be calculated using the following formulas with the internal inductance of the TSV included:

\[
R_T = R_{dc} + R_{ac} \quad (4)
\]

\[
L_T = L_{ext} + 2L_{int} \quad (5)
\]

where \( R_{dc} = \frac{2T_L}{\sigma_{dc} \pi (T_D / 2)^2} \), \( R_{ac} = \frac{2T_L \sqrt{\mu_0 \sigma_{ac} f}}{\pi} \) and \( L_{ext} = \frac{\mu_0 T_L}{\pi \cos \frac{\theta}{2} (T_D / T_D)} \), \( L_{int} = \frac{T_L}{2\pi T_D} \sqrt{\frac{\mu_0}{\pi \sigma_{ac} f}} \); \( L_{ext} \) is the overall loop inductance of the TSV pair when the current flows on the external surfaces only, and \( L_{int} \) denotes the internal inductance of the TSV that change with frequency. The \( R_T \) and \( L_T \) values calculated using (4) and (5) also agree well with the results obtained from the 2D cross-sectional analysis.

Finally, the modified lumped circuit model was simulated and the S-parameter results are compared with the 3D full wave simulation in Figure 5.
The results of the full wave simulation and the circuit model agree very well up to 20 GHz. Therefore, the modified circuit model is suitable to evaluate the electrical performance of the TSV in a lightly-doped silicon substrate.

III. MODELING OF TSV IN HEAVILY-DOPED SILICON SUBSTRATE

In practical applications, the doping density of the silicon substrate varies a lot, which will significantly influence the electrical performance of the TSV structure. In the following example, a heavily-doped silicon substrate with a conductivity of 100000 S/m, which is a typical value for digital applications, is used while all the other geometry parameters remain the same as the lightly-doped case. Similar to the lightly-doped case, a 3D full-wave simulation was performed and the E-field distribution is shown in Figure 6. The same excitations of 1V and -1V were applied across the two TSVs on the top and bottom surfaces, respectively.

According to the field distribution in Figure 6, there is current flowing in the vertical direction along the TSVs inside the highly doped silicon substrate. Since the silicon substrate now has a fairly large conductivity, it can be treated as a relatively good conductor. There still exists the coaxial capacitance between the TSV and the silicon substrate through the SiO₂ insulator layer. However, there is a looped E-field distribution between the two TSVs in this case, which corresponds to the loop current inside the silicon substrate, the lumped circuit model for the heavily-doped case is thus proposed as in Figure 7.

In the proposed lumped circuit model, C₁ corresponds to the coaxial capacitance between the TSV and the silicon substrate. Its value can be calculated by (1) which is 110.64 fF for our example. The circuit loop formed by R₀ and Rₛᵢ represents the current loop which is shown in the field distribution plot in Figure 6. Rₜ in this circuit model is the same as in the lightly-doped silicon substrate case while Lₜₒₜₐₜ is quite different. The difference is caused by the vertical direction current flowing in the highly doped silicon substrate. The inductance difference can be further explained using the circuit in Figure 8.
Since the structure is symmetric, the left part of the whole structure is taken as an example. In the lightly-doped case, there is no current $I_2$ in the silicon substrate. Thus, only $L_{ST}$, the self partial inductance associated with the TSV, and $M_T$, the mutual partial inductance between the two TSVs, exist and their combination leads to the total inductance $L_T$ in the lightly-doped case. However, in a heavily-doped silicon substrate, there is vertical current $I_2$. Therefore, $L_{Si}$, the self partial inductance associated with the silicon substrate, and $M_{s1}$, $M_{s2}$, the mutual partial inductances between the TSV and the substrate, must be taken into account and they influence the overall inductance $L_{Total}$.

In the proposed circuit model, $R_0$, $R_{Si}$, and $L_{Total}$ are difficult to evaluate. In this work, they were obtained by data fitting from the S-parameter results of the full-wave simulation. Further investigations are needed to obtain the analytical expressions in the future. Their fitted values are shown in (6) – (8) as:

$$R_0 = 20 \Omega$$  \hspace{1cm} (6) \\
$$R_{Si} = 2.77e^{-6}\sqrt{f} - 1.88e - 2(\Omega)$$  \hspace{1cm} (7) \\
$$L_{Total} = L_T - 2.44e - 17\sqrt{f} + 1.84e - 13(H)$$  \hspace{1cm} (8)

Using (6) – (8) and the proposed circuit model in Figure 7, the S-parameters of the TSV structure in the heavily-doped silicon substrate were calculated and the results are compared with the 3D full-wave simulation in Figure 9.

**REFERENCES**


