

Testing of the DS1822 VHDL Model

A variety of test benches were used to test proper functioning of the model. Tests were “white-box” in the sense that information internal to the model was checked in addition to information being sent or received from outside the DS1822 model. Every test bench begins with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the master followed by presence pulse(s) transmitted by the slave(s). Following is a description of each test bench.

- Test bench 1 (*testbench1.vhd*)

This test bench tests the Read Rom command followed by a Read Scratchpad function command. For these commands, there can be only one slave on the bus; so only one DS1822 is initialized in the test bench. The Read Rom command allows the master to read the slave’s 64-bit serial code and the Read Scratchpad command allows the master to read the contents of the scratchpad. In both of these commands, the data transfer starts with the least significant bit first. To verify that data has been read correctly, the bus master re-calculates the CRC (Cyclic Redundancy Check) from the received data. If a correct read has occurred, the CRC should be all 0s. Otherwise, the read operation must be repeated. For a detailed explanation of how CRC is calculated, please refer to the algorithm provided in Application Note 27 entitled “Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products”.

- Test bench 2 (*testbench2.vhd*)

This test bench tests the Match Rom command followed by the Read Power supply function command. Multiple slaves are initialized on the bus with different serial codes and the type of power supply used (external or parasite). The Match Rom command followed by a 64-bit serial code allows the bus master to address a specific slave on a multi-drop or single-drop bus. Only the slave that exactly matches the 64-bit serial code will respond to the function command issued by the master (in our case, a Read Power supply command); all other slaves on the bus will wait for a reset pulse. The bus master issues a read time slot after the Read Power supply command to determine the kind of power supply used by the DS1822. During the read time slot, a parasite powered DS1822 will pull the bus low and an externally powered DS1822 will let the bus remain high.

- Test bench 3 (*testbench3.vhd*)

This test bench tests the Search Rom command. The master identifies the ROM codes of all devices on the bus with the Search Rom command. The master learns the ROM codes through a process of elimination that requires the master to perform a Search Rom cycle (i.e., the Search Rom command followed by data transfer) as many times as necessary to identify all slave devices. Multiple slaves are instantiated with different serial codes. The ROM codes are stored in a variable *slaveID* and the number of slaves in a variable *index*.

- Test bench 4 (*testbench4.vhd*)

This test bench is mainly used to test the Alarm Search command, which allows the master to determine if any DS1822s experienced an alarm condition during the most recent temperature conversion. The Convert T function command is issued before the

Alarm Search command. The sequence of commands issued is Skip Rom, Convert T and Alarm Search. A Reset pulse is given before Skip Rom and Alarm Search. Four slaves are initialized on the bus. The temperature values supplied to the DS1822s are as follows

1. DUT1: 85° C this is in the specified range of -55° C to 125° C.
2. DUT2: 155° C this is out of the specified range.
3. DUT3: -56° C this is out of the specified range.
4. DUT4: 95° C this is in the specified range.

An alarm flag will be set for the second and third DS1822s after the Convert T, as the temperature is out of the specified range. When the master issues the Alarm Search command, only these DS1822s will respond. The ROM codes of the DS1822s responding to the alarm search are stored in a variable *slaveID* and the number responding is stored in a variable *index*.

- Test bench 5 (*testbench5.vhd*) & Test bench 6 (*testbench6.vhd*)

Test bench 5 and test bench 6 test the Convert T function command when using external and parasite power, respectively. A reset pulse and Skip Rom command is issued before a Convert T command in both test benches. Convert T initiates temperature conversion and the resulting thermal data is stored in the 2-byte temperature register in scratchpad memory. The values in the scratchpad are checked directly within the model (i.e. not using a ReadScratchpad command sequence). If the master issues a read-time slot during conversion when the DS1822 is externally powered (test bench 5), the DS1822 responds with a 0, indicating the temperature conversion is in progress. In parasite mode this notification technique cannot be used since the bus must be pulled high during the conversion.

- Test bench 7 (*testbench7.vhd*)

This test bench tests the Write Scratchpad function command. A reset pulse and Skip Rom command are given before the Write Scratchpad command. Write Scratchpad allows the master to write 3 bytes of data to the DS1822's scratchpad. These bytes should be written into the 2nd, 3rd and 4th bytes of the scratchpad. Values in the scratchpad are checked directly within the model.

- Test bench 8 (*testbench8.vhd*) & test bench 9 (*testbench9.vhd*)

Test bench 8 and test bench 9 test the Copy Scratchpad function command when the DS1822s use external and parasite power, respectively. A reset pulse and Skip Rom command are given before the Copy Scratchpad command. Copy Scratchpad copies the contents of the scratchpad T_H , T_L and configuration register (bytes 2, 3 and 4) to EEPROM. When the DS1822 is externally powered (test bench 8), the DS1822 will respond with a 0 if the master issues a read time slot during this operation, indicating the copy command is still in progress. In parasite mode this notification technique cannot be used since the bus is pulled high during copying.

- Test bench 10 (*testbench10.vhd*) & test bench 11 (*testbench11.vhd*)

These test benches test the Recall E^2 function command for DS1822s with external and parasite power supply, respectively. A reset pulse and Skip Rom command are given before Recall E^2 command. Recall E^2 recalls the alarm trigger values (T_H and T_L) and the configuration data from EEPROM and places the data in bytes 2, 3 and 4 of scratchpad

memory. The success of the Recall E² command is tested by directly observing the contents of the scratchpad within the model. If the master issues a read slot command to an externally powered DS1822 (test bench 10) while the Recall E² is in progress, the DS1822 responds with a 0, indicating that the recall is in progress.

- Test bench 12 (*testbench12.vhd*)

In this test bench, the transaction sequence required to access the DS1822 is violated. After the initialization sequence, a Function command is issued instead of a Rom command and vice-versa. The DS1822 should enter the *init* state and wait for a reset pulse. This operation is checked by directly observing the value of the internal current state signal *cs*.

- Test bench 13 (*testbench13.vhd*)

This test bench is used to check the response of the DS1822 when a reset pulse is given between the read/write operation. A Read Rom command is issued after a function command. A reset pulse is given during the read operation. The DS1822 should respond with a presence pulse. The Master then issues a Skip Rom followed by a Write Scratchpad command. A reset pulse is again given, but now in between the write operation. The DS1822 should again respond with a presence pulse.

- Test bench 14 (*testbench14.vhd*)

This test bench is used to check various timing constraints in the model: reset pulse less than 480 microseconds, recovery time less than 1 microsecond, and time slot more/less than 120/60 microseconds. All of these constraints are imposed in the test bench to check assert statements used in the model.

- Test bench 15 (*tb_example1.vhd*) & test bench 16 (*tb_example2.vhd*)

These test benches implement the examples given in the data sheets. In test bench 15, there are multiple DS1822s on the bus and they are using parasite power. The bus master initiates a temperature conversion in a specific DS1822 and then reads the scratchpad and recalculates the CRC to verify data. In test bench 16, there is only one DS1822 on the bus and it is using parasite power. The master writes T_H and T_L and configuration registers to the DS1822 scratchpad and then reads the scratchpad and recalculates the CRC to verify the data. The master then copies the scratchpad contents to EEPROM.