Bipolar Junction Transistor (BJT) chosen for this project was a 2N5210, npn - general purpose amplifier. Power supply used was 5V for the DC bias. Based on the power supply and typical characteristics of the BJT, $I_{ce}$ was to be between 1mA and 4mA. This region would have given high current gain at room temperature ($25^\circ$C), and it was high enough to provide decent swing around the Q-point.

![Figure 1: DC biasing characteristics](image)

Based on these values, $R_e$ and $R_c$ values were chosen. $R_c$ was 0.68 kΩ and $R_e$ was 0.39 kΩ. Thus,

![Figure 2: DC bias circuit](image)
After some calculations, standard resistors were chosen for $R_1$ and $R_2$ to be ___ There two resistors give Thevenin equivalent of ___, which was very close to the calculated (dered) value.

DC bias circuit was then built as shown in figure 2. DC parameters were then measured and shown in Table 1 (below).

<table>
<thead>
<tr>
<th>$V_c$</th>
<th>3.51 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_e$</td>
<td>0.838 V</td>
</tr>
<tr>
<td>$V_{ce}$</td>
<td>2.67 V</td>
</tr>
<tr>
<td>$V_b$</td>
<td>1.47 V</td>
</tr>
<tr>
<td>$I_{ca}$</td>
<td>2.163 mA</td>
</tr>
<tr>
<td>$I_{c}$</td>
<td>2.1704 mA</td>
</tr>
<tr>
<td>$I_{a}$</td>
<td>7.4 μA</td>
</tr>
</tbody>
</table>

Table 1 - Measured DC values (× - calculated)

From these, $\beta$ was calculated to be $\beta = 292$ and $r_e$ and $g_m$ were also obtained:

$$ r_e = \frac{V_t}{I_{c}} = 3.51 \, k\Omega $$

$$ g_m = \frac{I_c}{V_t} = 83.2 \, \text{mS} $$

The goal was to build an amplifier circuit with two coupling capacitors and an bypass condenser which was to control the lower cutoff frequency. The frequency value was 75 kHz.
Figure 3 - Full circuit simulation design

Figure 4 - Simulation Bode Plot
Simulation in Microcap was built as shown in Figure 3. Coupling capacitors used were large enough to be considered shorted for any small signal calculations. At the Bode plot shown in Figure 4, it was a good value to get a 3dB point had somewhat different values than what was measured, but the values were close to the ones obtained fused in the final circuit design. Small-signal circuit analysis was shown below:

\[
A_{V_{max}} = \frac{V_o}{V_i} = - g_m \cdot \frac{R_C \cdot R_e}{R_f} \cdot \frac{R_f \parallel R_b}{R_f \parallel (R_b + R_s)}
\]

\[
A_{V_{max}} = - g_m \cdot R_C \cdot \frac{R_f \parallel R_b}{R_f \parallel (R_b + R_s)} = -83.2 \frac{mV}{V} \cdot \frac{0.682 \text{mV}}{(3.51/10.17) \text{mV}} \cdot (3.51/10.17) + 50\Omega
\]

\[
A_{V_{max}} = -55.5
\]
Next, calculation of 3dB point, i.e. time constant related to it, was obtained. This time constant was then used to obtain value of the by-pass capacitor which would provide a 3dB low frequency cut-off at 75 Hz.

![Circuit Diagram]

**Figure 6 - Small-signal equivalent circuit**

As explained previously, coupling capacitors \(C_0\) and \(C_2\) were large enough to be considered shorted in the analysis. Also, \(R_2\) was considered large enough not to have much effect. \(R_s\) was small enough (50 nΩ), so it was ignored in order to make the calculation simpler.
Figure 7 - Voltage gain for emitter by-pass capacitor

Figure 7 showed the effects of the emitter by-pass capacitor. Therefore,

From these equations, it was easy to obtain $C_E$ which would give $\theta_m = 5V$

$C_E = 182.2 \mu F$ value was used in the circuit.

$\theta_m = C_E \cdot R_E = 180 \mu F \cdot 0.39 k\Omega = 70.2 \mu s$

$\Delta f = \frac{1}{2\pi \theta_m} = \frac{1}{2\pi \cdot 70.2 \times 10^{-3}} = 2.27 Hz$
Parasitic capacitance and high cutoff frequency were calculated below.

High cutoff frequency was measured to be lower, around 7 MHz, as shown in Figure 7. This could be explained by series resistance of the function generator output, which is 50 Ω. If this was included in the calculation, the Rs would then be 100 Ω total, and the fr would be 7.11 MHz. This would almost match the measured value. Simulation plot has shown value of 3.16 MHz, much lower than both, calculated and measured. Bode gain plot is shown in Figure 9.
Figure 9 - Voltage Gain Bode Plot