Report: Project #1

[redacted]

EE 254

Fall 2013

Bipolar junction transistor (BJT) chosen for this project was a 2N5210, npn - general purpose amplifier. Power supply used was 5V for the DC bias. Based on the power supply and typical characteristics of the BJT, I_{CQ} was to be between 1mA and 4mA. This region would have given high current gain at room temperature (25°C), and it was high enough to provide decent swing around the Q-point.

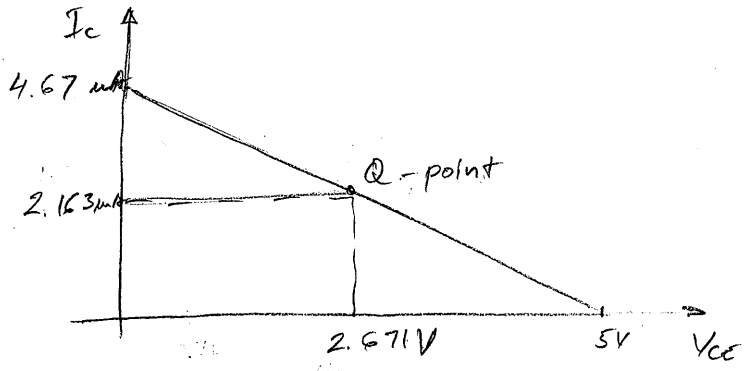

Figure 1 - DC biasing characteristics

Based on these values R_C and R_E values were chosen. R_C was 0.68kΩ and R_E was 0.39kΩ. Thus,

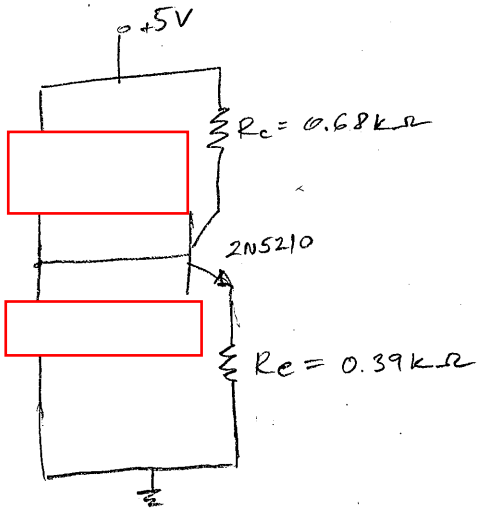

Figure 2 - DC bias circuit

After some calculations, standard resistors were chosen for R_1 and R_2 to be [redacted]. These two resistors give Thevenin equivalent of [redacted], which was very close to the calculated (desired) value.

DC bias circuit was then built as shown in figure 2. DC parameters were then measured and shown in table 1 (below).

V_C	3.51 V
V_E	0.838 V
V_{CE}	2.671 V
V_B	1.47 V
I_{CQ}	2.163 mA
I_{EQ}	2.1704 mA
I_{BQ} *	7.4 μA

Table 1 - Measured DC values (* - calculated)

From these, β was calculated to be $\beta = 292$ and r_π and g_m were also obtained:

$$r_\pi = \frac{V_T \cdot \beta}{I_{CQ}} = 3.51\,k\Omega \qquad g_m = \frac{\beta}{r_\pi} = 83.2\,\frac{mA}{V}$$

The goal was to build an amplifier circuit with two coupling capacitors and an bypass capacitor which was to control the lower cutoff frequency. The frequency value was 75 Hz.

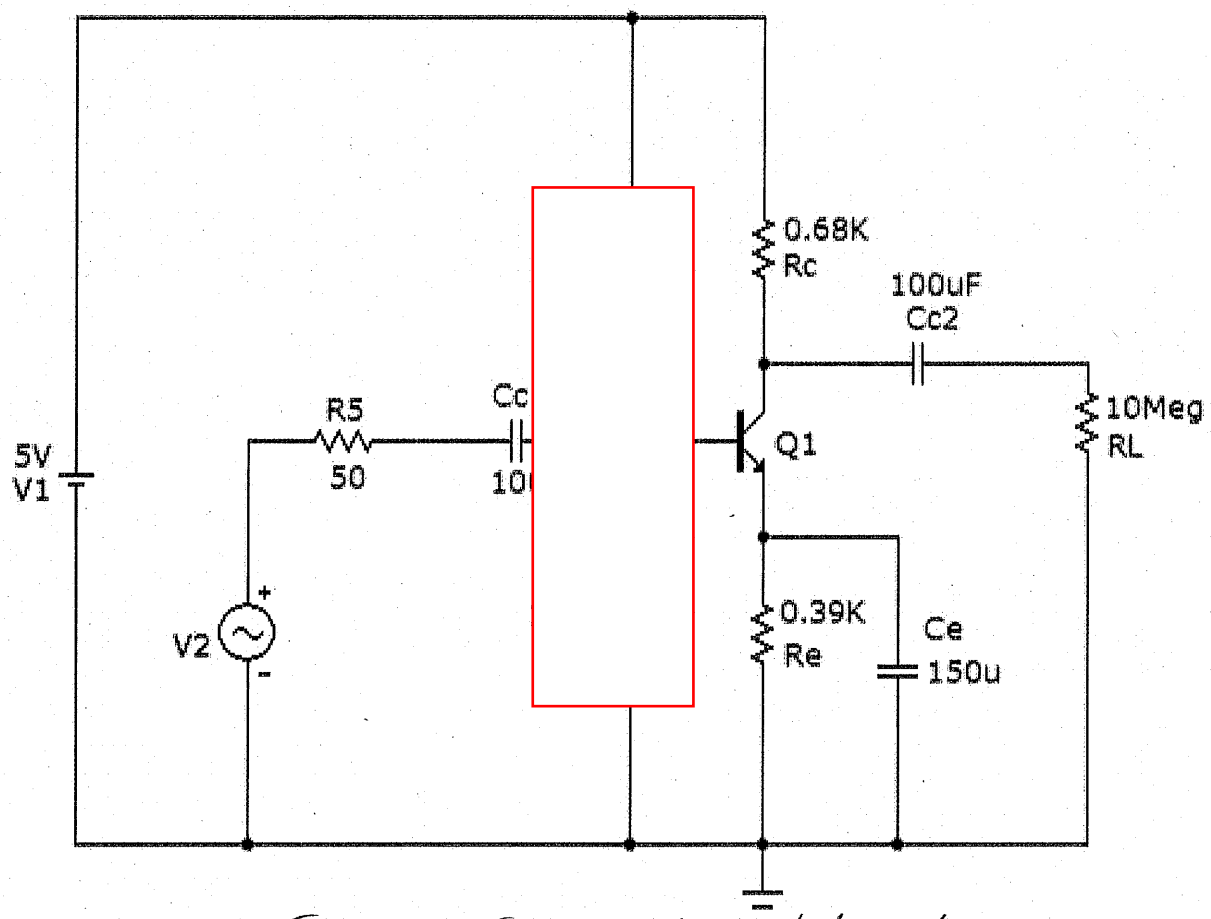

Figure 3 - Full circuit simulation design

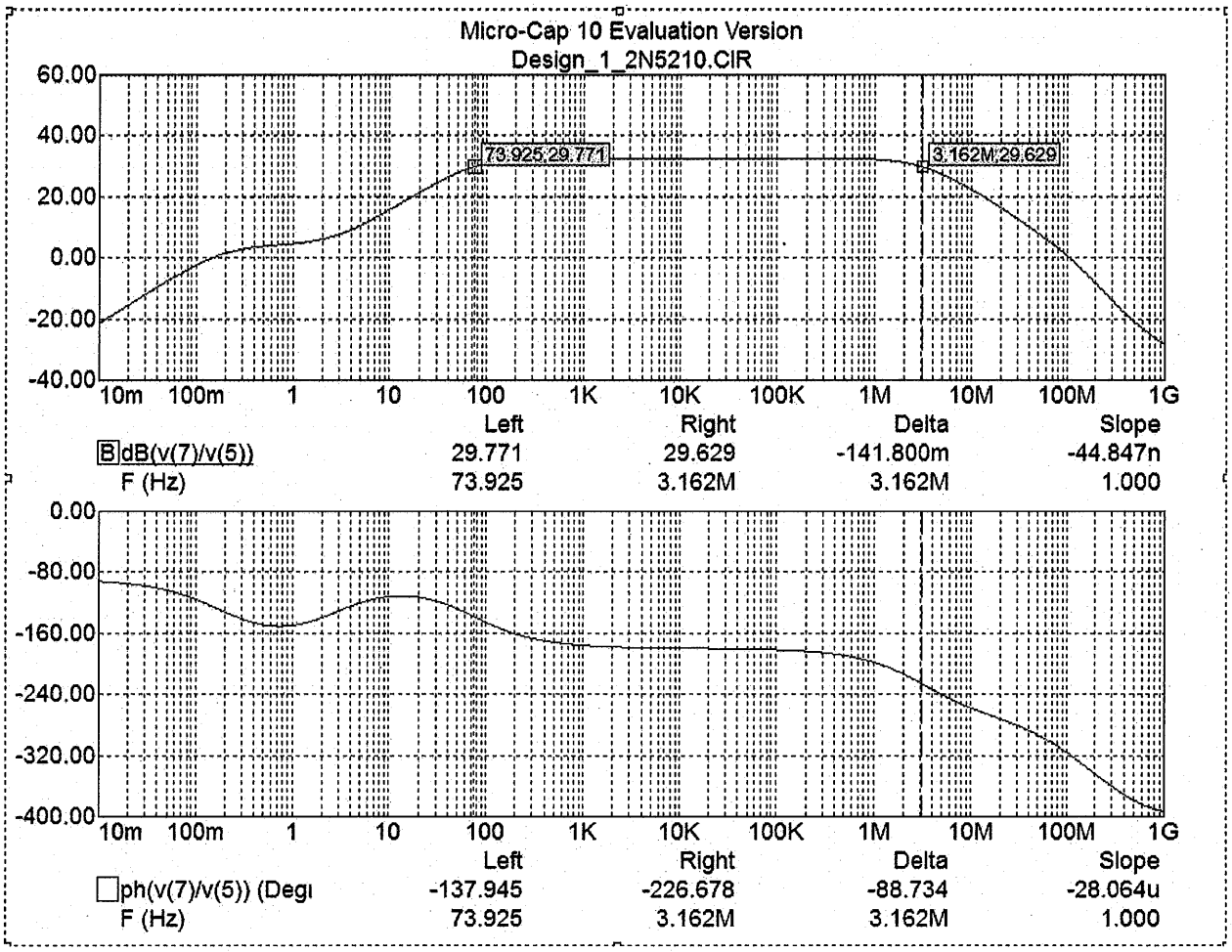

Figure 4 - Simulation Bode Plot

Simulation in Microcap was built as shown in figure 3. Coupling capacitors used were large enough to be considered shorted for any small signal calculations. As the Bode plot shows in figure 4, [redacted] was a good value to get a 3dB point had somewhat different values than what was measured, but the values were close to the ones obtained/used in the final circuit design.

Small-signal circuit analysis was shown below:

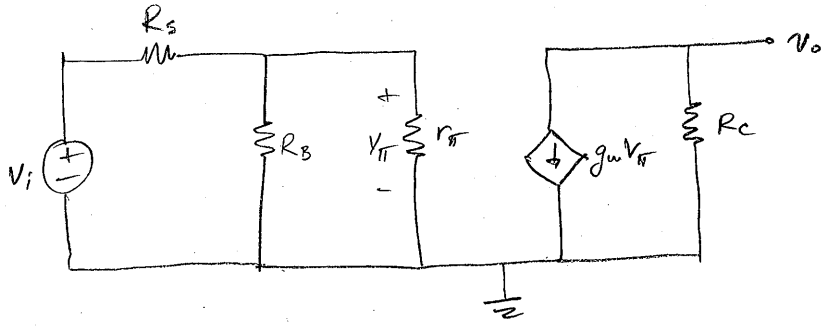

Figure 5 - Mid-band small-signal equivalent circuit

$$A_{V_{max}} = \frac{V_o}{V_i} = -\frac{g_m V_\pi \cdot R_C}{V_\pi} \cdot \frac{r_\pi \,//\, R_B}{r_\pi \,//\, R_B + R_S}$$

$$A_{V_{max}} = -g_m \cdot R_C \cdot \frac{r_\pi \,//\, R_B}{r_\pi \,//\, R_B + R_S} = -83.2\frac{mA}{V} \cdot 0.68k\Omega \cdot \frac{(3.51 \,//\, 10.17)k\Omega}{(3.51 \,//\, 10.17)k\Omega + 50\Omega}$$

$$A_{V_{max}} = -55.5$$

Next, calculation of 3dB point, i.e. time constant related to it, was shown. This time constant was then used to obtain value of the by-pass capacitor which would provide a 3dB low-frequency cut-off at 75Hz.

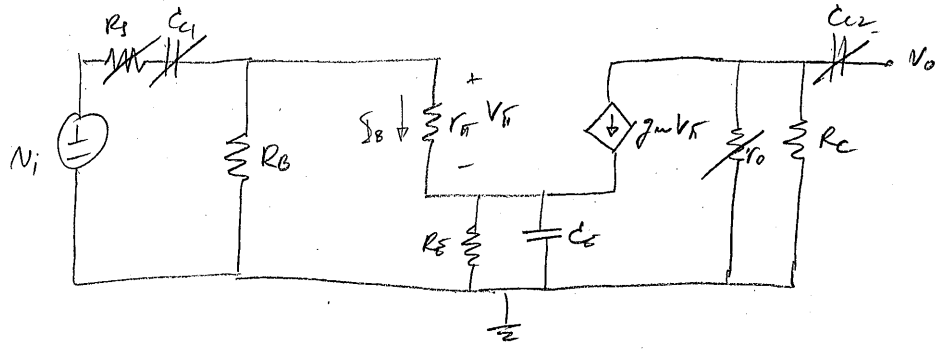

Figure 6 - Small-signal equivalent circuit

As explained previously, coupling capacitors C_{c1} and C_{c2} were large enough to be considered shorted in the analysis. Also, r_o was considered large enough not to have much effect. R_s was small enough (50Ω), so it was ignored in order to make the calculation simpler.

$$r_\pi + (1+\beta) R_E$$

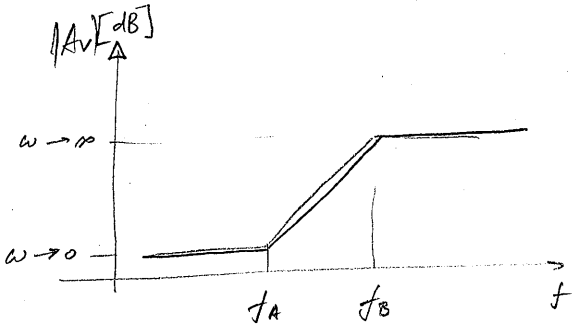

Figure 7 - Voltage gain for emitter by-pass capacitor

Figure 7 showed the effects of the emitter by-pass capacitor. Therefore,

From these equations it was easy to obtain C_E which would give

$C_E = 182.2\mu F$ value was used in the circuit.

$$\tau_A = C_E \cdot R_E = 180\mu F \cdot 0.39 k\Omega = 70.2 ms$$

$$f_A = \frac{1}{2\pi \tau_A} = \frac{1}{2\pi \cdot 70.2 \times 10^{-3}} = 2.27 Hz$$

• $V_{cc} = 5V$

Figure 8 - Final circuit design

Parasitic capacitance and high cutoff frequency were calculated below.

High cutoff frequency was measured to be lower, around 7 MHz, as shown in figure 9. This could be explained by series resistance of the function generator output, which is 50Ω. If this was included in the calculation, the R_s would then be 100Ω total, and the f_H would be 7.14MHz. This would almost match the measured value. Simulation plot has shown value of 3.16MHz. Much lower than both, calculated and measured. Bode gain plot is shown in figure 9.

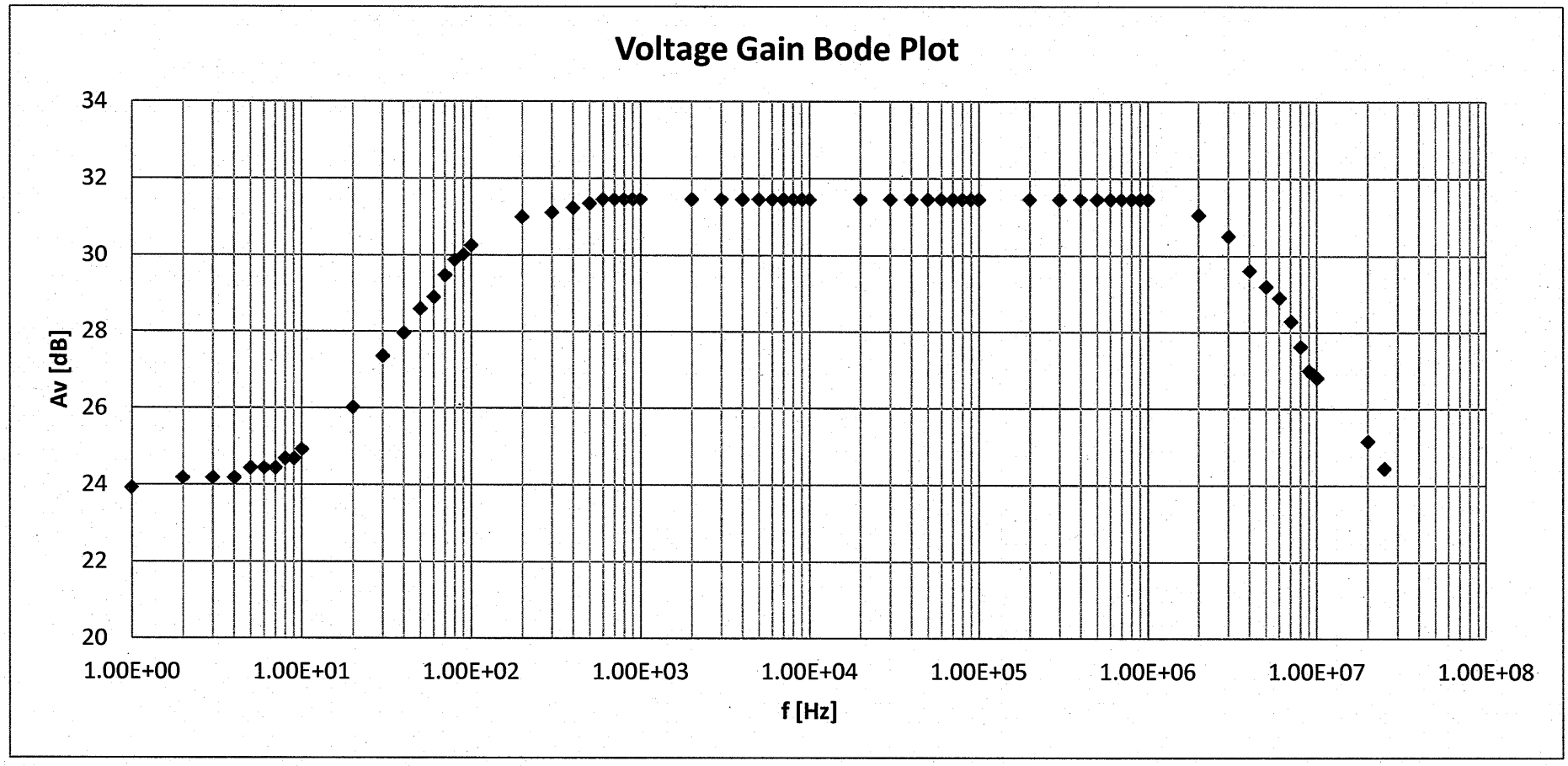

Figure 9 - Voltage gain Bode plot