Project 1: CE Amplifier

Introduction:
The purpose of this project was to design a common emitter amplifier circuit. The transistor had to be npn, not from the lab and available from newark.com. The criteria to be met included that the circuit must be bias stable, must have AC gain stability and an emitter bypass capacitor, must have an undistorted output, must have suitable coupling capacitors that meet my assigned lower cutoff frequency of 60Hz.

Experiment:
To begin the design, I looked through the available transistors on newark.com, and chose the 2N5551 npn transistor for my amplifier. After comparing it with some other transistors it seemed to have values that would match most closely to my input voltage (5V at 10kHz and 10kHz). 5V were chosen for the ease of calculations.

Next I chose $I_c = 1mA$ for simplicity of design.
For the AC analysis (Figure 2), I calculated $g_m$ (calculation 9), and $A_v$ (calculation 10). Next, I needed to find the values of the coupling capacitors and bypass capacitor. To calculate $C_e$, I rearranged the equation to calculate frequency (calculation 11), whose $f$ was my lower cutoff frequency of 60 Hz. Since $C_e$ was to be the dominating capacitor, it was necessary to choose a frequency much lower than 60 Hz to ensure that the coupling capacitors would not interfere with $C_e$. I chose a frequency of 0.04 Hz for $C_e$, and 0.006 Hz for $C_{c2}$. This ensured values that were available in the lab, and that the capacitors would not dominate the circuit (calculations 12-13).

After building and testing the circuit, I measured the current and voltage values to compare (Table 1). Recalculating gave $\beta_a = 16.275438$, which was used along with other measured values for another set of calculations.

Next, the upper and lower cutoff frequencies were measured using the oscilloscope (figures 3 and 4). The midband gain was in that range (figure 5). The gain was calculated to be $1.11 \times 10^{-4} = 64.966$. After getting these values, the parameters $C_t$, $C_m$, and $C_{c2}$ were calculated to see how the calculated upper cutoff frequency compared to the measured upper cutoff frequency (calculations 14-18). To do this, SPICE parameters were used to find $C_t$, $C_m$, and $C_{c2}$. After calculating $S_\text{iso}$ be 3.5844 MHz, it was much larger than the measured 4 kHz. Since $R_5$ was the only estimated value, it must be skewing the data.
somehow. Using an Excel spreadsheet, Rs was increased until the gain was lowered and the cutoff frequency was lowered to very close to my measured cutoff frequency. That value was 525 KHz, using a 523-Ω resistor connected in series between the circuit and frequency generator; the upper and lower cutoff frequencies were measured (Figure 6-7). My new upper cutoff frequency was 362 KHz, and the new lower cutoff frequency was 47.4 Hz. The voltage and current parameters were measured again to compare (Table 2). The gain was reduced to 1.94/V/30.1V = 50.9186, which is still relatively good: β increased to 181.596, which is OK, because the two calculated were within 15 of each other.

Next, the BJT SPICE parameters were calculated again for comparison (calculations 19-22). This increased Cm by 1.0039 times.

Conclusion.

It is possible to control both the gain and the midband with an amplifier circuit. I was able to use a chosen lower cutoff frequency and calculate the values of both bypass and coupling capacitors to cause this cutoff. Controlling the high end cutoff was trickier, but I was able to adjust Rs to an appropriate number that did not change my original value very much. When recalculating the C1, C2, and Cm parameters, I did not get the expected cutoff frequency. This is probably due to an error in calculation.
because the upper cutoff frequency increased. The fault was not in the circuit itself, because my measured values were very similar when comparing Tables 1 and 2. It would be interesting to see if there is a formula to find Rs given a cutoff frequency instead of trying to adjust it. Increasing Rs definitely helped, but there should be a better way to find that value apart from trial and error. Rs also adjusted the lower cutoff frequency as well, internal resistance can be a big issue in cases like this.
AC Analysis:

Capacitor Calculations:

1) \( C_E = \)
Capacitor Calculations (cont.):

1. \( C_{e_1} \)

Choose \( f_c = 0.60 \text{Hz} \)

\[
T_{S_1} = (R_S + R_{TH} / \eta) C_{e_1}
\]

12) \( C_{e_1} = \boxed{160 \mu F} \)

13) \( 2 \pi f_c e_2 (K e_1 K_2) \)
14) c

15) c

16) C_M

17) $t_p = \frac{C_M}{\sqrt{L/R_M}} = \frac{C_M}{\sqrt{L/R_M}}$

\[ t_p = \left( \frac{C_M}{\sqrt{L/R_M}} \right) \left( \frac{R_{th}/R_S}{1/\xi} \right) = 4.44 \times 10^{-8} \text{s} \]

18) $f_H = \frac{1}{2\pi t_p} = \frac{1}{2\pi t_p} = 3.844 \text{ MHz}$
Figures and Tables

Figure 1: DC Common Emitter Circuit

Figure 2: AC equivalent
Figure 5: Midband Gain region

Figure 6: Upper cutoff frequency after changing Rs
**Power Discrete Bipolar Electrical Parameter**

**Power Amplifier Transistor**

**Product: 2N5551 / TO-92**

```
.MODEL 2N5551 npn
+ IS  = 2.04174E-14  BF  = 122.7  NF  = 1
+ BR  = 17.075      NR  = 1      ISE = 5.7544E-13
+ NE  = 2          ISC = 2.29087E-11 NC  = 1.5
+ VAF = 176.831     VAR = 35.3    IKF = 0.144627
+ IKR = 0.0158489   RB  = 125     RBM = 8.092
+ IRB = 1.12202E-7  RE  = 0.14    RC  = 1.8
+ CJE = 2.450889E-11 VJE = 0.7175263 MJE = 0.3413777
+ FC  = 0.5         CJC = 5.03462E-12 VJC = 0.5
+ M3C = 0.3226407   XTB = 1.2776   EG  = 1.2222
+ XTI = 3           TF  = 1.73E-11
```

* Creation: Sep.-24-2004
* Fairchild Semiconductor

Table 3: Fairchild 2N5551 SPICE model
2N5551 - MMBT5551
NPN General Purpose Amplifier

Features
- This device is designed for general purpose high voltage amplifiers and gas discharge display drivers.
- Suffix "-C" means Center Collector in 2N5551 (1. Emitter 2. Collector 3. Base)
- Suffix "-Y" means $I_{FE} 180-240$ in 2N5551 (Test condition: $I_C = 10mA, V_{CE} = 5.0V$)

Absolute Maximum Ratings * $T_J = 25^\circ C$ unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
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<tbody>
<tr>
<td>$V_{CEO}$</td>
<td>Collector-Emitter Voltage</td>
<td>160</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CBO}$</td>
<td>Collector-Base Voltage</td>
<td>180</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EBO}$</td>
<td>Emitter-Base Voltage</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>$I_C$</td>
<td>Collector current - Continuous</td>
<td>600</td>
<td>mA</td>
</tr>
<tr>
<td>$T_J, T_{Stg}$</td>
<td>Junction and Storage Temperature</td>
<td>-55~+150</td>
<td>°C</td>
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* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:
1. These ratings are based on a maximum junction temperature of 150 degrees C.
2. These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics $T_J=25^\circ C$ unless otherwise noted

<table>
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<th>Symbol</th>
<th>Parameter</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
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<tr>
<td>$P_D$</td>
<td>Total Device Dissipation</td>
<td></td>
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<td></td>
<td>Derate above 25°C</td>
<td>625</td>
<td>mW</td>
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<tr>
<td></td>
<td></td>
<td>5.0</td>
<td>mW/°C</td>
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<tr>
<td>$R_{JJA}$</td>
<td>Thermal Resistance, Junction to Case</td>
<td>83.3</td>
<td>°C/W</td>
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<tr>
<td>$R_{JJA}$</td>
<td>Thermal Resistance, Junction to Ambient</td>
<td>200</td>
<td>°C/W</td>
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</table>

* Device mounted on FR-4 PCB 1.6" x 1.6" x 0.06"
Typical Performance Characteristics

Figure 1. Typical Pulsed Current Gain vs Collector Current

Figure 2. Collector-Emitter Saturation Voltage vs Collector Current

Figure 3. Base-Emitter Saturation Voltage vs Collector Current

Figure 4. Base-Emitter On Voltage vs Collector Current

Figure 5. Collector Cutoff Current vs Ambient Temperature

Figure 6. Input and Output Capacitance vs Reverse Voltage
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<th>Definition</th>
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<td>This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.</td>
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