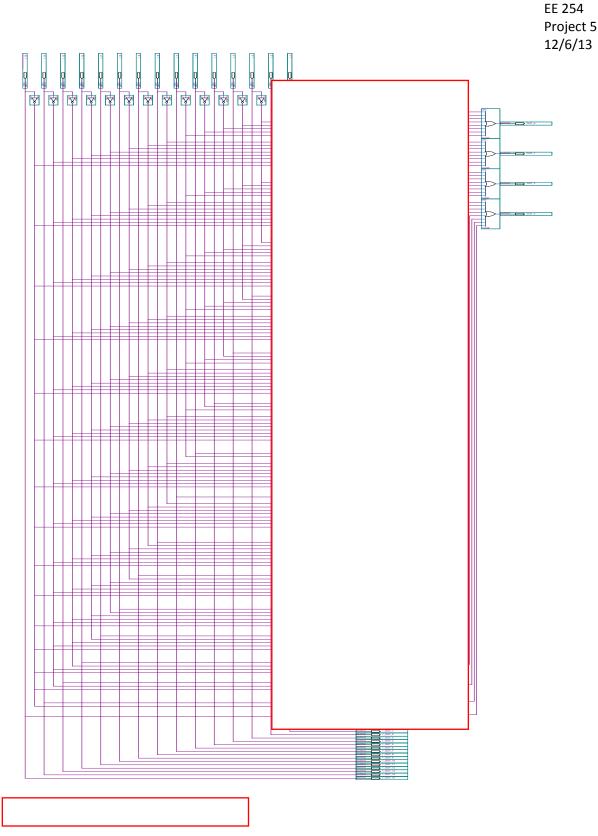


Figure 3: voltage outputs



After building the circuit, the voltage of each level was measured in order to compare to the calculated levels (table 2 and figures 5-6). Then, the priority encoder was downloaded to the Altera board, and the

outputs of the circuit were connected to the expansion header on the Altera board. The pin assignments were made, and as the voltage increased, the 4 logic levels increased in order.

Logic level	Trial 1 (V)	Trial 2 (V)
0000	0	0
0001	0.17758	0.1718
0 0 10	0.49732	0.48038
0011	0.78455	0.82613
0 100	1.13348	1.16044
0 101	1.4524	1.4051
0 110	1.7228	1.7277
0 111	2.0955	2.1036
1000	2.3584	2.4575
1001	2.7118	2.6591
1010	2.9829	2.9771
1011	3.3469	3.282
1100	3.6028	3.6346
1101	3.9735	3.9271
1110	4.2247	4.268
1111	4.5616	4.6434

## Table 2: minimum voltage required for each logic level

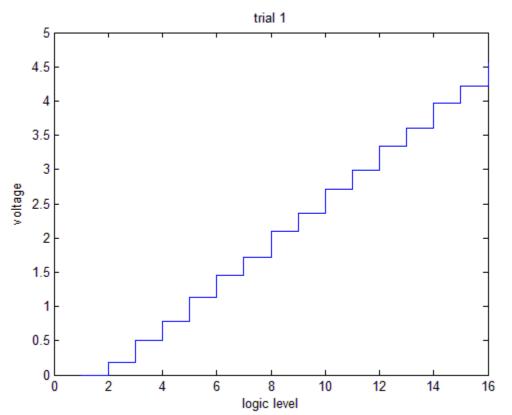
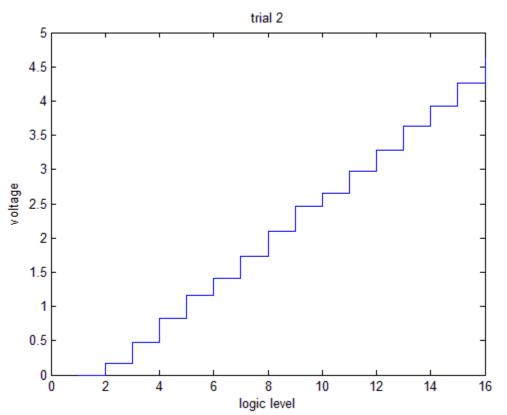


Figure 5: plot of voltage increase

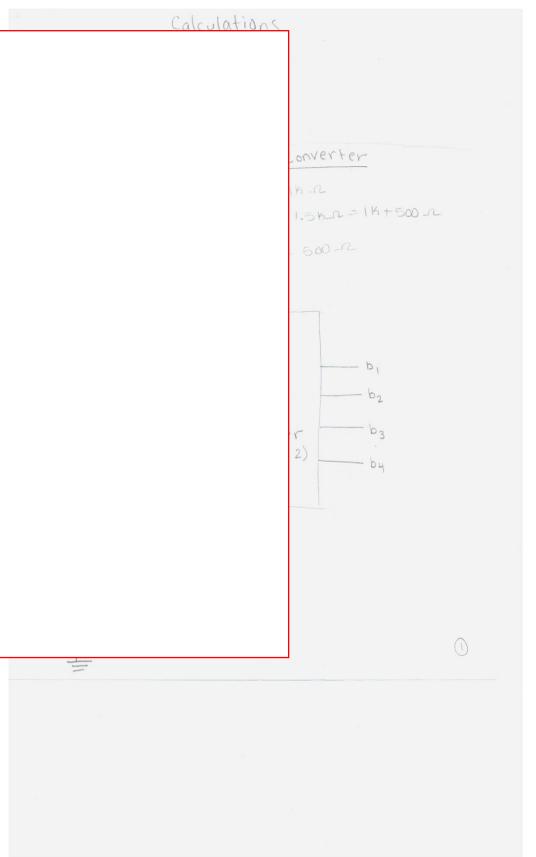


## Figure 6: plot of voltage increase trial 2

## Conclusion

This experiment re reference voltage is analog voltage is s the comparator wi smallest voltage le voltage levels are s resistors are deter the circuit, it work

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2

$$\begin{aligned} V_{15} &= \frac{29V_{ref}}{16} = 4.53125V \\ V_{14} &= \frac{27V_{ref}}{16} = 4.21875V \\ V_{13} &= \frac{25V_{ref}}{16} = 3.90625V \\ V_{12} &= \frac{23V_{ref}}{16} = 3.59375V \\ V_{12} &= \frac{21V_{ref}}{16} = 3.28125V \\ V_{10} &= \frac{19V_{ref}}{16} = 2.96875V \\ V_{q} &= \frac{17V_{ref}}{16} = 2.65625V \\ V_{q} &= \frac{15V_{ref}}{16} = 2.34375V \\ V_{q} &= \frac{15V_{ref}}{16} = 2.03125V \\ V_{5} &= \frac{9V_{ref}}{16} = 1.71875V \\ V_{5} &= \frac{9V_{ref}}{16} = 1.40625V \\ V_{5} &= \frac{9V_{ref}}{16} = 1.40625V \\ V_{3} &= \frac{V_{ref}}{16R}(3R+R_{2}) = \frac{5V_{ref}}{16} = 1.09375V \\ V_{3} &= \frac{V_{ref}}{16R}(2R+R_{2}) = \frac{5V_{ref}}{32} = 0.46875V \\ V_{2} &= \frac{V_{ref}}{16R}(\frac{R}{2}) = \frac{3V_{ref}}{32} = 0.46875V \\ V_{1} &= \frac{V_{ref}}{16R}(\frac{R}{2}) = \frac{V_{ref}}{32} = 0.15625V \end{aligned}$$

-> Vref = 5V