Project 5: D/A and A/D Converters


Figure 3: voltage outputs


After building the circuit, the voltage of each level was measured in order to compare to the calculated levels (table 2 and figures 5-6). Then, the priority encoder was downloaded to the Altera board, and the
outputs of the circuit were connected to the expansion header on the Altera board. The pin assignments were made, and as the voltage increased, the 4 logic levels increased in order.

| Logic <br> level | Trial 1 <br> $(\mathbf{V})$ | Trial 2 <br> $(\mathbf{V})$ |
| :---: | :---: | :---: |
| 0000 | 0 | 0 |
| 0001 | 0.17758 | 0.1718 |
| 0010 | 0.49732 | 0.48038 |
| 0011 | 0.78455 | 0.82613 |
| 0100 | 1.13348 | 1.16044 |
| 0101 | 1.4524 | 1.4051 |
| 0110 | 1.7228 | 1.7277 |
| 0111 | 2.0955 | 2.1036 |
| 1000 | 2.3584 | 2.4575 |
| 1001 | 2.7118 | 2.6591 |
| 1010 | 2.9829 | 2.9771 |
| 1011 | 3.3469 | 3.282 |
| 1100 | 3.6028 | 3.6346 |
| 1101 | 3.9735 | 3.9271 |
| 1110 | 4.2247 | 4.268 |
| 1111 | 4.5616 | 4.6434 |

Table 2: minimum voltage required for each logic level


Figure 5: plot of voltage increase


Figure 6: plot of voltage increase trial 2


EE 254
Project 5
12/6/13


$$
\begin{aligned}
& V_{15}=\frac{29 V_{\text {ret }}}{16}=4.53125 \mathrm{~V} \\
& V_{14}=\frac{27 V_{\text {ret }}}{16}=4.21875 \mathrm{~V} \\
& V_{13}=\frac{25 \mathrm{~V}_{\text {ret }}}{16}=3.90625 \mathrm{~V} \\
& V_{12}=\frac{23 \mathrm{Vret}}{16}=3.59375 \mathrm{~V} \\
& V_{11}=\frac{21 V_{\text {ret }}}{16}=3.28125 \mathrm{~V} \\
& V_{10}=\frac{19 V_{\text {ref }}}{16}=2.96875 \mathrm{~V} \\
& V_{9}=\frac{17 V_{\text {ref }}}{16}=2.65625 \mathrm{~V} \\
& V_{8}=\frac{15 V_{\text {ret }}}{16}=2.34375 \mathrm{~V} \\
& V_{7}=\frac{13 V_{\text {ret }}}{16}=2.03125 \mathrm{~V} \\
& V_{6}=\frac{11 V_{\text {ref }}}{16}=1.71875 \mathrm{~V} \\
& V_{5}=\frac{9 V_{\text {ret }}}{16}=1.40625 \mathrm{~V} \\
& V_{4}=\frac{V_{\text {ret }}}{16 R}\left(3 R+R_{2}\right)=\frac{7 \mathrm{~V}_{\text {ret }}}{16}=1.09375 \mathrm{~V} \\
& V_{3}=\frac{V_{\text {ret }}}{16 R}(2 R+2 / 2)=\frac{5 V_{\text {ret }}}{32}=0.78125 \mathrm{~V} \\
& V_{2}=\frac{V_{\text {ret }}}{16 R}(R+R / 2)=\frac{3 \mathrm{~V} \text { ret }}{32}=0.46875 \mathrm{~V} \\
& V_{1}=\frac{V_{\text {ref }}}{16 R}\left(\frac{R}{2}\right)=\frac{V_{\text {ref }}}{32}=0.15625 \mathrm{~V} \\
& V_{\text {ref }}=5 \mathrm{~V}
\end{aligned}
$$

