## 8-Bit R-2R Digital to Analog Converter

| Circuit sh <br> tolerance. <br> was obtai <br> was used <br> the breadr <br> they were <br> collected <br> was obtai <br> actual val <br> During th <br> increased <br> absorb th <br> was concl <br> explain th <br> 2 shows tl <br> larger. | sistors with low <br> y other binary value |
| :--- | :--- |
| utput. A dip switch |  |
| witched manually on |  |
| oltage values $\left(V_{0}\right)$ then |  |
| al and expected values |  |
| alog output voltages |  |
| both expected and |  |

The experiment yielded good results as the calculated percentage errors fell below $1 \%$ in all but one of the randomly obtained binary values.


Figure 1: Digital to analog converter circuit.

## Expected values and error calculation


3. For the decimal value of 93 which is 01011101 in binary:


## Experimental and expected values and plots

| $\begin{gathered} \text { Digital } \\ \text { In } \end{gathered}$ | Expected Vout | Actual Vout | $\begin{aligned} & \text { Digital } \\ & \text { In } \end{aligned}$ | Expected Vout | Actual Vout | $\begin{gathered} \text { Digital } \\ \text { In } \end{gathered}$ | Expected Vout | Actual Vout |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0.002174 | 85 | 4.6816 | 4.7038 | 171 | 9.4184 | 9.4225 |
| 1 | 0.0551 | 0.05858 | 87 | 4.7918 | 4.8141 | 173 | 9.5285 | 9.5285 |
| 3 | 0.1652 | 0.17015 | 89 | 4.9020 | 4.925 | 175 | 9.6387 | 9.6396 |
| 5 | 0.2754 | 0.27996 | 91 | 5.0121 | 5.0344 | 177 | 9.7488 | 9.7532 |
| 7 | 0.3855 | 0.3905 | 93 | 5.1223 | 5.143 | 179 | 9.8590 | 9.8629 |
| 9 | 0.4957 | 0.50171 | 95 | 5.2324 | 5.2525 | 181 | 9.9691 | 9.9727 |
| 11 | 0.6059 | 0.61296 | 97 | 5.3426 | 5.367 | 183 | 10.0793 | 10.0823 |
| 13 | 0.7160 | 0.7217 | 99 | 5.4527 | 5.4777 | 185 | 10.1895 | 10.1911 |
| 15 | 0.8262 | 0.83184 | 101 | 5.5629 | 5.5845 | 187 | 10.2996 | 10.301 |
| 17 | 0.9363 | 0.9456 | 103 | 5.6730 | 5.6951 | 189 | 10.4098 | 10.407 |
| 19 | 1.0465 | 1.0561 | 105 | 5.7832 | 5.8082 | 191 | 10.5199 | 10.5076 |
| 21 | 1.1566 | 1.1654 | 107 | 5.8934 | 5.9166 | 193 | 10.6301 | 10.6106 |
| 23 | 1.2668 | 1.2759 | 109 | 6.0035 | 6.0271 | 195 | 10.7402 | 10.7003 |
| 25 | 1.3770 | 1.3986 | 111 | 6.1137 | 6.137 | 197 | 10.8504 | 10.7934 |
| 27 | 1.4871 | 1.5132 | 113 | 6.2238 | 6.2493 | 199 | 10.9605 | 10.8852 |
| 29 | 1.5973 | 1.6068 | 115 | 6.3340 | 6.36 | 201 | 11.0707 | 10.972 |
| 31 | 1.7074 | 1.7167 | 117 | 6.4441 | 6.4682 | 203 | 11.1809 | 11.0546 |
| 33 | 1.8176 | 1.8338 | 119 | 6.5543 | 6.578 | 205 | 11.2910 | 11.139 |
| 35 | 1.9277 | 1.9487 | 121 | 6.6645 | 6.6894 | 207 | 11.4012 | 11.2292 |
| 37 | 2.0379 | 2.052 | 123 | 6.7746 | 6.7999 | 209 | 11.5113 | 11.3125 |
| 39 | 2.1480 | 2.1624 | 125 | 6.8848 | 6.907 | 211 | 11.6215 | 11.387 |
| 41 | 2.2582 | 2.2784 | 127 | 6.9949 | 7.017 | 213 | 11.7316 | 11.457 |
| 43 | 2.3684 | 2.3937 | 129 | 7.1051 | 7.0852 | 215 | 11.8418 | 11.5423 |
| 45 | 2.4785 | 2.493 | 131 | 7.2152 | 7.1946 | 217 | 11.9520 | 11.6156 |
| 47 | 2.5887 | 2.6034 | 133 | 7.3254 | 7.3022 | 219 | 12.0621 | 11.6833 |
| 49 | 2.6988 | 2.7162 | 135 | 7.4355 | 7.433 | 221 | 12.1723 | 11.7614 |
| 51 | 2.8090 | 2.8275 | 137 | 7.5457 | 7.5474 | 223 | 12.2824 | 11.8433 |
| 53 | 2.9191 | 2.9363 | 139 | 7.6559 | 7.6578 | 225 | 12.3926 | 11.93 |
| 55 | 3.0293 | 3.0464 | 141 | 7.7660 | 7.7658 | 227 | 12.5027 | 11.982 |
| 57 | 3.1395 | 3.1583 | 143 | 7.8762 | 7.8758 | 229 | 12.6129 | 12.044 |
| 59 | 3.2496 | 3.2688 | 145 | 7.9863 | 7.9882 | 231 | 12.7230 | 12.109 |
| 61 | 3.3598 | 3.3765 | 147 | 8.0965 | 8.0981 | 233 | 12.8332 | 12.17 |
| 63 | 3.4699 | 3.4793 | 149 | 8.2066 | 8.2074 | 235 | 12.9434 | 12.242 |
| 65 | 3.5801 | 3.6005 | 151 | 8.3168 | 8.3172 | 237 | 13.0535 | 12.31 |
| 67 | 3.6902 | 3.7115 | 153 | 8.4270 | 8.43 | 239 | 13.1637 | 12.38 |
| 69 | 3.8004 | 3.8213 | 155 | 8.5371 | 8.5412 | 241 | 13.2738 | 12.448 |
| 71 | 3.9105 | 3.9315 | 157 | 8.6473 | 8.6468 | 243 | 13.3840 | 12.489 |
| 73 | 4.0207 | 4.0429 | 159 | 8.7574 | 8.7562 | 245 | 13.4941 | 12.566 |
| 75 | 4.1309 | 4.1524 | 161 | 8.8676 | 8.8716 | 247 | 13.6043 | 12.646 |
| 77 | 4.2410 | 4.2622 | 163 | 8.9777 | 8.9822 | 249 | 13.7145 | 12.696 |
| 79 | 4.3512 | 4.3719 | 165 | 9.0879 | 9.0901 | 251 | 13.8246 | 12.77 |
| 81 | 4.4613 | 4.4835 | 167 | 9.1980 | 9.1995 | 253 | 13.9348 | 12.842 |
| 83 | 4.5715 | 4.5941 | 169 | 9.3082 | 9.3125 | 255 | 14.0449 | 12.95 |

Table 1: Input decimal values converted to binary and used to obtain the analog output voltage

```
clear all
close all
clc
[v,T,vT] = xlsread('Data_1.xlsx');
D_input = v(:,1);
A_out = v(:,2);
[v,T,vT] = xlsread('Data_2.xlsx');
D_input2 = v(:,1);
A_out2 = v(:,2);
figure
hold on
plot(D_input, A_out, 'r')
hold on
stairs(D_input2, A_out2, 'b')
```



Figure 2: Plots of expected values and the actual values.


Figure 3: Plots of expected values and the actual values zoomed in.

