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LECTURE - 34

Ex

n JFET

$I_{DSS} = 2mA$ $\quad V_P = -3.5V$

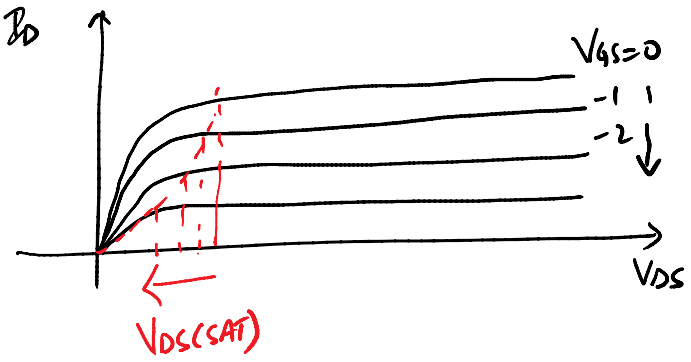
I_D ? $\quad V_{DS(SAT)}$ FOR $V_{GS} = 0, \frac{V_P}{4}, \frac{V_P}{2}$

SAT. REGION

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2m\left(1 - \frac{V_{GS}}{-3.5}\right)^2$$

$$V_{DS(SAT)} = V_{GS} - V_P = V_{GS} - (-3.5)$$

V_{GS}	I_D	$V_{DS(SAT)}$
0	2mA	3.5V
$V_P/4$	1.13mA	2.63V
$V_P/2$	0.5mA	1.75V



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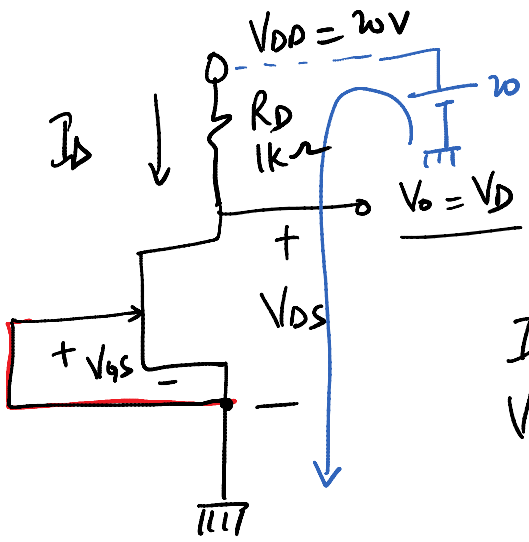
Ex

BJT ACTIVE REGION OF ASSUMPTION



$I_{DSS} = 10mA$

$V_P = -4V$

I_D ?

V_{DS} ?

① $R_D = 1K\Omega$ GATE CONNECTED TO SOURCE

$\therefore V_{GS} = 0\ V$

REGION OF OPERATION ??

ASSUME IN SATURATION !

$V_{GS} = 0 \Rightarrow I_D = I_{DSS} = 10mA$

KVL D-S LOOP

$-V_{DS} + I_D(1K) + V_D = 0$

$V_D = V_{DS} = 20 - (10m)(1K) = 10V$

$V_{DS(SAT)} = V_{GS} - V_P = 0 - (-4) = 4V$

$V_{DS} > V_{DS(SAT)}$

$10V > 4V$ → ASSUMPTION IS CORRECT TRANSISTOR IS IN SAT.

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(2)

$R_D = 1.8k\Omega$

ASSUME IN SAT. REGION

$V_{GS}=0 \Rightarrow I_D = I_{DSS} = 10mA$

KVL D-S LOOP

$V_{DS} = V_D = V_{DD} - (10m)(1.8k\Omega) = 2V$

$V_{DS(SAT)} = 4V$

SINCE $V_D = V_{DS} < V_{DS(SAT)}$ $\therefore$ TRANSISTOR IS IN THE TRIODE REGION

$$I_D = I_{DSS}\left[2\left(1-\frac{V_{GS}}{V_P}\right)\left(\frac{V_{DS}}{-V_P}\right) - \left(\frac{V_{DS}}{V_P}\right)^2\right]$$

$$= 10m\left[2\left(1-\frac{0}{-4}\right)\left(\frac{V_{DS}}{4}\right) - \left(\frac{V_{DS}}{-4}\right)^2\right]$$

$$I_D = 10m\left[\frac{V_{DS}}{2} - \frac{V_{DS}^2}{16}\right] \quad \cdots \quad (1)$$

KVL D-S LOOP

$V_{DS} = 20 - I_D(1.8K)$

$$I_D = \frac{20 - V_{DS}}{1.8K} \quad \cdots \quad (2)$$

(2) IN (1)

$$\frac{20 - V_{DS}}{} = 10m\left[\frac{V_{DS}}{2} - \frac{V_{DS}^2}{10}\right]$$

$$\frac{20 - V_{DS}}{1.8K} = 10m \left[\frac{V_{DS}}{2} - 10 \right]$$

$$\frac{1}{16} V_{DS}^2 - 10V_{DS} + 20 = 0$$

$$V_{DS} = \frac{10 \pm \sqrt{100 - 90}}{2.25}$$

$$V_{DS} = 3.039 \checkmark, \quad \cancel{5.55V}$$

$$\therefore V_{DS} = 3.039V$$

$$I_D = \frac{20 - 3.039}{1.8K} = 9.423\,mA$$

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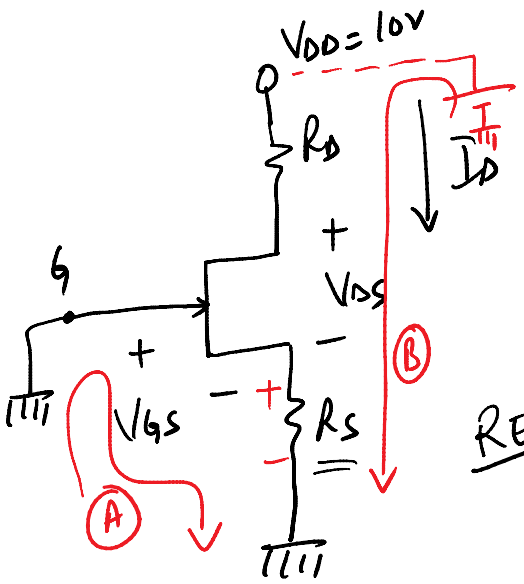
DESIGN



$I_{DSS} = 5mA$

$V_P = -4V$

READ $I_D = 2mA$

$V_{DS} = 6V$

ASSUME TR. IS IN SAT.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$2m = 5m\left[1 - \frac{V_{GS}}{-4}\right]^2$$

$$V_{GS} = -1.47V$$

KVL loop A

$$V_{GS} + I_D R_S = 0$$

$$R_S = -\frac{V_{GS}}{I_D} = -\frac{(-1.47)}{2m} = 0.735k\Omega$$

KVL D-S loop → (B)

$$-V_{DD} + I_D R_D + V_{DS} + I_D R_S = 0$$

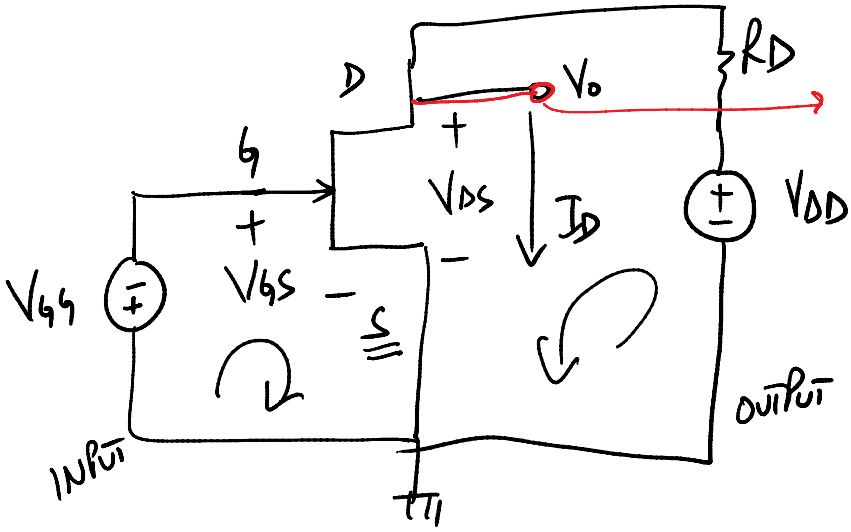
$$R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D} = \frac{10 - 6 - (2m)(0.735K)}{2m}$$

$$= 1.27k\Omega$$

$V_{DS(SAT)} = V_{GS} - V_P = -1.47 - (-4) = 2.53V$

$V_{DS} = 6V > V_{DS(SAT)}$ ∴ TR. IS IN SAT.

COMMON SOURCE JFET CIRCUIT



KVL G-S LOOP

$$V_{GS} = -V_{GG}$$ [NEGATIVE VALUE]

SAT. REGION $V_{DS} > V_{DS(SAT)}$

$$V_{DS(SAT)} = V_{GS} - V_P$$ [POSITIVE VALUE]

$I_{DS} = I_D$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

KVL D-S LOOP

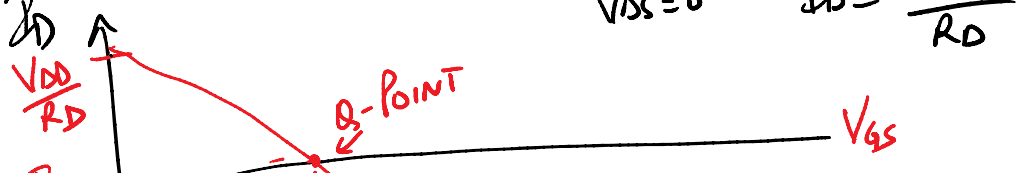
$$-V_{DD} + I_D R_D + V_{DS} = 0$$

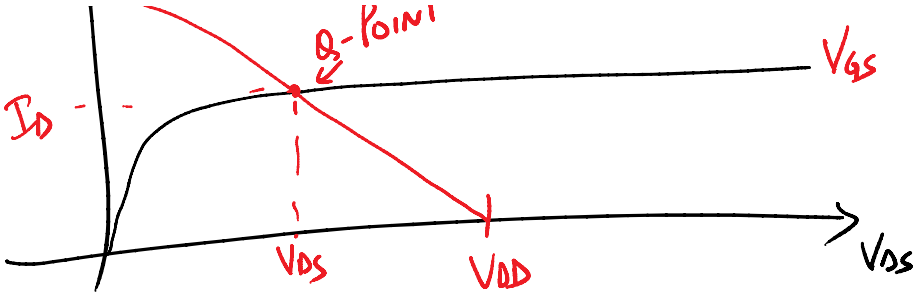
$$\boxed{V_{DS} = V_{DD} - I_D R_D}$$ → LOAD LINE EQUATION

INTERCEPTS

$I_D = 0$ $\quad V_{DS} = V_{DD}$

$V_{DS} = 0$ $\quad I_D = \frac{V_{DD}}{R_D}$




Q-POINT
I_D
V_{GS}
V_{DS}
V_{DD}
V_{DS}

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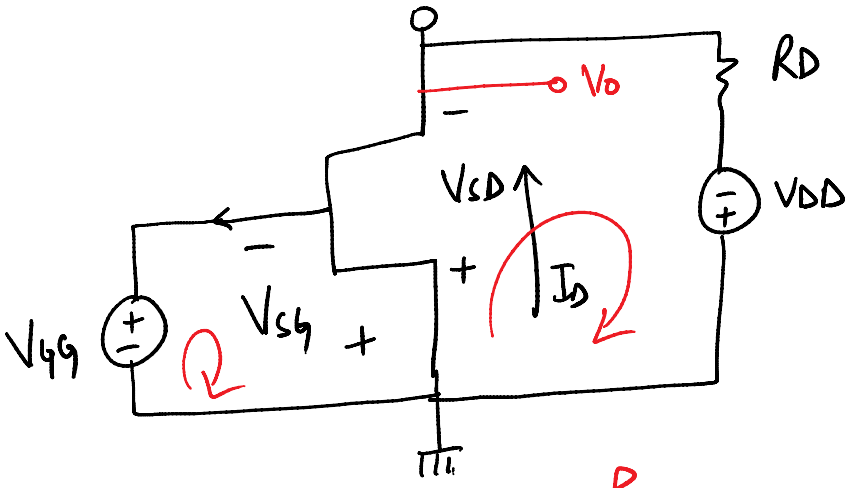
P JFET



KVL G-S LOOP

$$-V_{GG} - V_{SG} = 0$$

$$V_{SG} = -V_{GG} \quad \text{[NEGATIVE VALUE]}$$

$$V_{GS} = V_{GG} \quad \text{[POSITIVE VALUE]}$$

ASSUME OP. IS IN SAT. REGION

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

KVL D-S LOOP

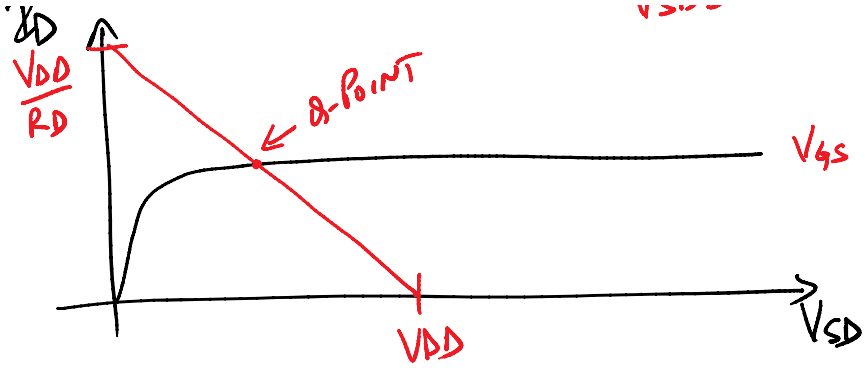
$$V_{SD} + I_D R_D - V_{DD} = 0$$

$$V_{SD} = V_{DD} - I_D R_D \rightarrow \text{LL EQUATION}$$

$$V_{SD(SAT)} = V_P - V_{GS}$$

$I_D = 0 \quad V_{SD} = V_{DD}$

$V_{SD} = 0 \quad I_D = \frac{V_{DD}}{R_D}$


VDD
RD
Q-POINT
VGS
VDD
VSD

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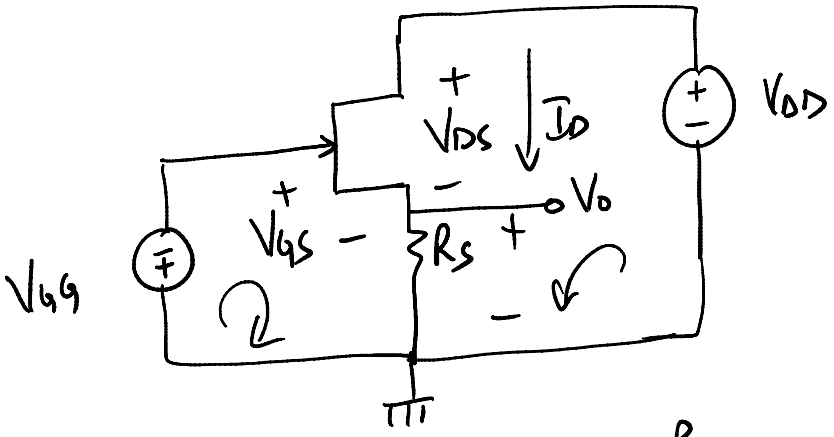
SOURCE FOLLOWER CIRCUIT



KVL G-S LOOP

$$V_{GG} + V_{GS} + I_D R_S = 0$$

$$V_{GS} = -V_{GG} - I_D R_S$$

[SHOULD BE NEGATIVE]

OPERATION IS IN SAT. REGION

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

KVL D-S LOOP

$$V_{DS} = V_{DD} - I_D R_S$$

$$V_O = I_D R_S = I_{DSS} R_S \left[1 - \frac{V_{GS}}{V_P}\right]^2$$

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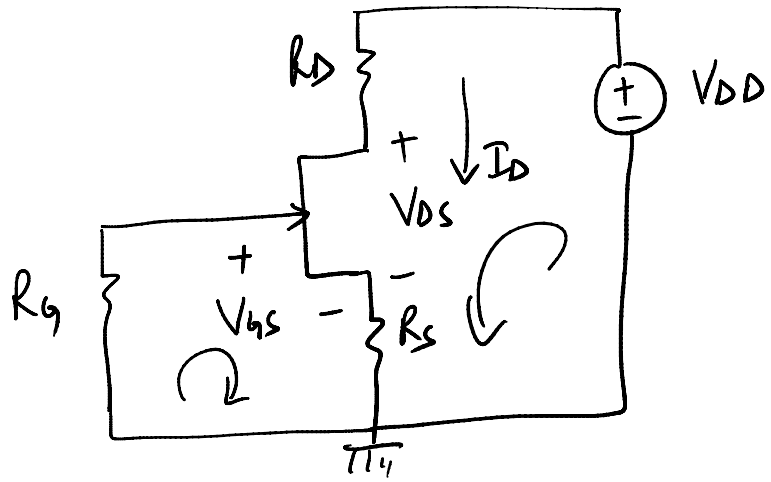
SELF BIASING JFET CIRCUIT



SINCE NO SOURCE ON GATE SIDE

$I_G = 0A$

$\therefore$ KVL GS LOOP

$V_{GS} + I_D R_S = 0$

$V_{GS} = -I_D R_S$ [NEGATIVE VALUE]

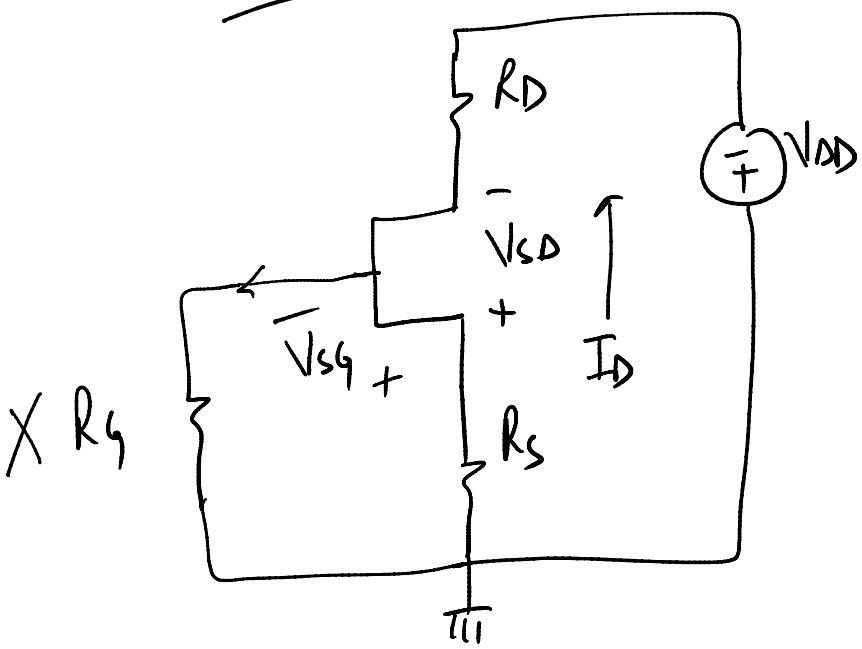
OP. IS IN SAT. REGION

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

KVL D-S LOOP

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

P-JFET



KVL G-S LOOP

$$I_D R_S + V_{SG} = 0$$

$$V_{SG} = -I_D R_S$$

$$V_{GS} = I_D R_S \quad \text{[POSITIVE VALUE]}$$

OP. IN SAT. REGION

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

KVL D-S LOOP

$$V_{SD} = V_{DD} - I_D (R_D + R_S)$$